Control of Parallel Connected Modular Multilevel Converters

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Abstract: The modular multilevel converter (MMC) is an emerging and highly attractive multilevel converter topology for high-voltage and high-power applications. This paper proposes the control method of parallel-connected modular multilevel converters (parallel-MMCs), which assumes that the multiple MMCs are directly connected at both ac and dc sides to effectively enhance the power rating as expected. Two key problems were first solved for the parallel-MMCs under the normal operation conditions: voltage balancing of sub-modules and mitigation of circulating currents, where the novel transformed third-order harmonic resonant controller in the synchronous reference frame was employed to mitigate the dominant second-order and fourth-order circulating currents and a sixth-order harmonic resonant controller is used to attenuate the zero-sequence sixth-order circulating current existed in all phase currents per MMC. Considering the high risk of switch fault in the parallel-MMCs, the fault-tolerant operation schemes were then proposed in this paper to address the major concerns of open-circuit and short-circuit switch fault in a sub-module, respectively. Carefully controlling the healthy sub-modules and the corresponding phase arms, the parallel-MMCs can successfully maintain their balanced capacitor voltages and mitigate the circulating currents with the qualified output waveform obtained. In addition, the parallel configuration of MMCs provides the unique solution for the short-circuit switch fault operation which was seldom discussed in the published literature works with respect to the MMC fault-tolerant operation schemes. MATLAB simulations and the constructed experimental prototype have verified the performance of the proposed control strategy.

Keywords: MMC, Speed Drives, AC, DC.

1. INTRODUCTION

A. Inverter

The Inverter is an electrical device which converts direct current (DC) to alternate current (AC). The inverter is used for emergency backup power in a home. The inverter is used in some aircraft systems to convert a portion of the aircraft DC power to AC. The AC power is used mainly for electrical devices like lights, radar, radio, motor, and other devices.

B. Multilevel Inverter

Now a day’s many industrial applications have begun to require high power. Some appliances in the industries however require medium or low power for their operation. Using a high power source for all industrial loads may prove beneficial to some motors requiring high power, while it may damage the other loads. Some medium voltage motor drives and utility applications require medium voltage. The multi level inverter has been introduced since 1975 as alternative in high power and medium voltage situations. The Multi level inverter is like an inverter and it is used for industrial applications as alternative in high power and medium voltage situations. Types of Multilevel Inverter:

Multilevel inverters are three types.
1. Diode clamped multilevel inverter
2. Flying capacitors multilevel inverter
3. Cascaded H-bridge multilevel inverter

1. Diode Clamped Multilevel Inverter

The main concept of this inverter is to use diodes and provides the multiple voltage levels through the different phases to the capacitor banks which are in series. A diode transfers a limited amount of voltage, thereby reducing the stress on other electrical devices. The maximum output voltage is half of the input DC voltage. It is the main drawback of the diode clamped multilevel inverter. This problem can be solved by increasing the switches, diodes, capacitors. Due to the capacitor balancing issues, these are limited to the three levels.

Fig1. 5-level diode clamped multilevel inverter.
This type of inverters provides the high efficiency because the fundamental frequency used for all the switching devices and it is a simple method of the back to back power transfer systems. Ex: 5- Level diode clamped multilevel inverter, 9-level diode clamped multilevel inverter.

- The 5- level diode clamped multilevel inverter uses switches, diodes; a single capacitor is used, so output voltage is half of the input DC.
- The 9- level diode clamped multilevel inverter uses switches, diodes; capacitors are two times more than the 5-level diode clamped inverters. So the output is more than the input.

Applications of Diode Clamped Multilevel Inverter:
- Static var compensation
- Variable speed motor drives
- High voltage system interconnections
- High voltage DC and AC transmission lines

2. Flying Capacitors Multilevel Inverter

The main concept of this inverter is to use capacitors. It is of series connection of capacitor clamped switching cells. The capacitors transfer the limited amount of voltage to electrical devices. In this inverter switching states are like in the diode clamped inverter. Clamping diodes are not required in this type of multilevel inverters. The output is half of the input DC voltage. It is drawback of the flying capacitors multi level inverter. It also has the switching redundancy within phase to balance the flying capacitors. It can control both the active and reactive power flow. But due to the high frequency switching, switching losses will takes place. EX: 5-level flying capacitors multilevel inverter, 9-level flying capacitors multilevel inverter. This inverter is same like that diode clamped multi inverter, in this inverter only switches and capacitors are used.

Applications of Cascaded H-Bridge Multilevel Inverter:
- Motor drives, Active filters, Electric vehicle drives DC power source utilization Power factor compensators Back to back frequency link systems Interfacing with renewable energy resources.
- Advantages of Multilevel Inverter:

Fig2. 5-Level Flying Capacitors Multilevel Inverter.

Fig3. 5- H-bridge multi level inverter.
consists of two arms, which are named as the positive arm and the negative arm, respectively. The buffer inductors $L_s$ limit the circulating currents among six phase-legs in the parallel-MMCs. The general control diagram of parallel-MMCs for grid-tied applications is illustrated in Fig. 3, where the general control function is realized by the voltage-balancing control blocks and circulating current suppression control (CCSC) blocks for MMC 1 and MMC 2 and the external ZSCC control block. The decoupled current control block is assumed to generate the fundamental control reference in the grid-tied applications, which may vary depending on the application cases. A general three-phase PLL is assumed to obtain the phase angle, which is not drawn in Fig. 3. In what follows, we will illustrate the capacitors voltage balancing control method in detail, whose control principle is suitable for the parallel-MMCs operated under both the normal operation condition and the switch fault-tolerant operation conditions.

This paper proposes a novel CCSC method to suppress the three-phase second-, fourth-, and sixth-order circulating current harmonics by only using three resonant controllers with the precise circulating current harmonics tuning capability and the significant reduction of calculation burden as well. For tuning multiple harmonics, although the resonant controllers placed in the stationary reference frame can be used, they would result in more terms for summation. Therefore, as an alternative, the resonant controllers in the synchronous reference frame would be more effective, since each represents two equivalent resonant terms in the stationary reference frame for compensating two harmonics simultaneously as stated in. According to the circulating currents analysis in addition to the low-frequency component, the dc and high-frequency components also appear in the circulating currents. It has also been pointed out that the circulating currents only contain the even-order harmonics without the odd order harmonics. Especially, the second-, fourth-, and sixth-order harmonics dominate the circulating currents. She et al. employed many resonant controllers to suppress the second-, fourth-, and sixth-order circulating harmonics of the three-phase MMC and Zhang et al. assumed the repetitive controller to attenuate the circulating current harmonics per phase.

Fig. 4. Block diagrams of (a) individual voltage control and (b) average voltage control.

### III. INTERNAL CCSC

As a result of the SM capacitor voltage variation, the three parallel connected phase legs as shown in Fig. 1 may have different summed voltages. Consequently, this leads to the circulating currents among the three-phase units. The circulating currents will flow through the six-phase arms and distort the sinusoidal arm currents introducing the additional converter losses; therefore, the circulating current will threaten the safe operation of the power devices and capacitors. In addition, this current will influence the SM voltages and the output voltages as illustrated in Section II. The internal circulating currents analysis has been reported in the technical literature works. The authors in and analyzed the mechanism of three-phase circulating currents in the MMC and discussed the relationship between the amplitudes of the circulating currents and the parameters of the arm inductors. Although increasing the arm inductance can reduce the circulating currents, it is not able to completely eliminate the circulating currents and it is not practical due to the large inductor size and the high cost. An effective control method to eliminate the circulating currents was proposed in and . However, this method just suppressed the second-order harmonic current that appeared in the circulating currents. According to the circulating currents analysis in addition to the low-frequency component, the dc and high-frequency components also appear in the circulating currents. It has also been pointed out that the circulating currents only contain the even-order harmonics without the odd order harmonics. Especially, the second-, fourth-, and sixth-order harmonics dominate the circulating currents. She et al. employed many resonant controllers to suppress the second-, fourth-, and sixth-order circulating harmonics of the three-phase MMC and Zhang et al. assumed the repetitive controller to attenuate the circulating current harmonics per phase.

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Fig. 5. Block diagram of internal CCSC.
resonant controllers to, respectively, tune the transformed \( dq \) components under the synchronous reference frame as shown in Fig. 5. In order to suppress the sixth-order zero-sequence current harmonic, an additional resonant controller is assumed to suppress the summed three-phase current in Fig. 5. The assumed resonant controllers can be, respectively, written as

\[
G(s) = \frac{K_3 s}{s^2 + (\omega_0)^2}
\]

\[
G(s) = \frac{K_6 s}{s^2 + (3\omega_0)^2}
\]

The summed control signal per SM in the positive-arm and the negative-arm can be written as where \( v_j px \) and \( v_j nx \) \((x = a, b, \text{ or } c, j = 1 \text{ or } 2)\) are the primary control commands derived from the current control block in Fig. 3, whose detailed control diagram is drawn in Fig. 6, where the three-phase control signals \( v_j px \) and \( v_j nx \) will be assigned to control six arms per MMC to track the current reference.

IV. ANALYSIS AND CONTROL OF EXTERNAL ZSCCS IN PARALLEL-MMCs

The SM can be treated as a controlled voltage source when building the average model of parallel-MMCs. According to the analysis in [16], \( px1 \) and \( nx1 \) \((x = a, b, \text{ or } c)\) are the virtual equi potential points in Fig. 2. Therefore, both buffer inductors per phase can be treated as the parallel connected inductors in Fig. 7, where it is easy to obtain \( L1 = LS1 / 2, L2 = LS2 / 2 \). The sum of capacitor voltages in positive arm and negative arm per phase are equivalent to the controlled voltage \( U_j px \) and \( U_j nx \) \((x = a, b, \text{ or } c \text{ and } j = 1 \text{ or } 2)\).

Assuming that the equivalent switching frequency is much larger than the output voltage fundamental frequency, the parallel-MMCs can be further equivalent to a controlled voltage source viewed from its ac side, therefore, the equivalent average model of parallel-MMCs can be drawn as Fig. 8. The zero-sequence duty-cycle \( S_j z \) can be defined as

\[
S_j z = \frac{1}{2} S_j^p + \frac{1}{3} S_j^m + \frac{1}{3} S_j^n
\]

where

\[
d_j^p = \frac{1}{2} S_j^p - \frac{1}{3} S_j^m, d_j^m = \frac{1}{2} S_j^m - \frac{1}{3} S_j^n, d_j^n = \frac{1}{2} S_j^n - \frac{1}{3} S_j^p.
\]

As a result, the average model of parallel-MMCs with the zero-sequence components added is drawn in Fig. 9, where the ZSCC flowing in MMC 1 and MMC 2 are denoted by \( i01 \) and \( i02 \), respectively. Hence, the ZSCC \( i0 \) can be defined as

\[
i0 = i01 = i_a + i_b + i_c = -i02
\]

With the prerequisite of balanced SM voltages, the ZSCC \( i0 \) can be calculated by summing the three-phase currents of a single MMC as expressed in (8). Therefore, it is reasonable to suppress the external ZSCC only in one MMC to achieve the full elimination of ZSCC between the parallel-MMCs as that reported for controlling the parallel-connected two-level converters. A simple PI controller is assumed to control the ZSCC to be zero as shown in Fig. 3, where the generated modulation signals will be added to \( v1 pxi \) and \( v1 nxi \) to produce the final modulation signals for MMC 1.
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V. FAULT-TOLERANT OPERATION OF PARALLEL MMCS

In view of the high amount of power semiconductors in the parallel-MMCS, any failure can cause large downtime and tremendous losses for the consumers. Therefore, it is important to develop the fault-tolerant operation schemes to enhance the reliability. This paper proposes the novel PWM compensation schemes for the fault-tolerant operation of parallel-MMCS without using an additional backup hardware. Only single-switch fault in one SM is considered in this paper, whose failure conditions can be broadly classified as the open-circuit fault and short-circuit fault. Carefully analyzing the switching states per SM in Fig. 1, it is noted that the open-circuit fault of IGBT 1 and the short-circuit fault of IGBT 2 are identical for the fault-tolerant operation and similarly the short-circuit fault of IGBT 1 and the open-circuit fault of IGBT 2 are identical either in terms of their complementary switching sequence. Therefore, the fault-tolerant operation of parallel-MMCS only needs to consider two cases: open-circuit fault and short-circuit fault of IGBT1.

A. PWM Compensation Schemes for the Open-Circuit Fault-Tolerant Operation of IGBT 1

Once the IGBT 1 suffers the open-circuit fault, the whole SM is recommended to only output state \( \{0\} \) by keeping IGBT 2 ON in order to maintain the continuous arm current being equivalent to the bypass function of SMs. In this case, the corresponding phase arm will lose one voltage level. In order to reduce the circulating current induced by the absence of one SM, it is suggested that the corresponding opposite phase arm downgrade its switching level from \( N + 1 \) to \( N \) either. The healthy SM capacitor voltages in the faulty phase-leg should be slightly increased to \( \frac{NUc}{N} \) so that the summed phase voltage is still equal to \( NUc \) the same as that of other two healthy phase-legs. Doing so, the revised switching states in the faulty phase-leg would not induce any additional circulating current in theory. The switching level reduction in the faulty phase-leg can increase the output harmonics induced by the unbalanced output line voltages. Reducing the switching level of other five healthy phase-legs with or without increasing their SM capacitor voltages can keep the balanced output line voltage as an alternative.

![Harmonics spectrum and THD of line-voltages between phase A and B for the cases of (a) two SMs per arm in phase A and three SMs per arm in phase B (red) and two SMs per arm in phase A and B (blue) with switching frequency of 2000 Hz and (b) nine SMs per arm in phase A and ten SMs per arm in phase B (red) and nine SMs per arm in phase A and B (blue) with switching frequency of 500 Hz.](image)

Fig.9. Average model of parallel-MMCS with zero-sequence components added.

Fig.10. Harmonics spectrum and THD of line-voltages between phase A and B for the cases of (a) two SMs per arm in phase A and three SMs per arm in phase B (red) and two SMs per arm in phase A and B (blue) with switching frequency of 2000 Hz and (b) nine SMs per arm in phase A and ten SMs per arm in phase B (red) and nine SMs per arm in phase A and B (blue) with switching frequency of 500 Hz.
load current flowing loop resulting in the damageable overvoltage breakdown. Therefore, when such short-circuit failure happens, the corresponding whole phase arm should be shut down to protect the equipment. Traditionally, the single three-phase MMC cannot continue its normal operation since one phase-leg is out of operation. But fortunately, the parallel-MMCS provide the redundant phase-leg to ride-through the short-circuit failure condition with the careful consideration of tradeoff between the current rating and the output power.

As a consequence, the parallel-MMCS will continue its operation by only using five phase-legs. In order to maintain the symmetrical three-phase output currents, the corresponding phase leg in the healthy MMC can generate double output current with the output current of other four legs unchanged to produce the same output power as that before the switch failure. For example, assuming that the total three-phase output currents are \( i_a, i_b, \) and \( i_c \), respectively, and an SM of phase A in MMC 1 suffers the IGBT 1 short-circuit failure condition, the phase A in MMC 2 would produce the output current of \( i_a \), while the other four healthy phases would generate \( 12 i_b, 12 i_c, 12 i_b \), and \( 12 i_c \), respectively, as usual to make sure that the total three-phase currents are symmetrical as expected. In this case, the desired output currents per MMC are unbalanced. Therefore, the traditional decoupled positive-sequence current control method for the grid-tied applications illustrated in Fig. 6 cannot be solely employed to control the output currents since the unbalanced three-phase currents per MMC can be decomposed into the positive-sequence, negative-sequence, and zero-sequence components.

A combined closed-loop current controller is shown in Fig. 11, where the positive-sequence, negative-sequence, and zero-sequence components \( i_{x+j}, i_{x-j}, \) and \( i_{x0} (x = a, b \text{ or } c, j = 1 \text{ or } 2) \) are derived using (9). In order to use the positive-sequence decoupled current control method to control the desired zero-sequence output current, (10) further revises the zero-sequence components. Doing so, the zero-sequence current can be controlled using the similar positive-sequence decoupled current control block as shown in Fig. 11. Besides, the negative sequence current can be controlled using the negative-sequence decoupled current control block as shown in Fig. 12.
Fig14. Proposed Model of Modular Multilevel Converter.

Fig15. phase instantaneous active and reactive power of grid.

The circuit parameters are listed in Table I, where the output filter inductances are different. The d- and q-axis current references $i_d$ and $i_q$ in Fig. 6 are set to be 30 and 30 A, respectively, under both the normal and switch fault operation conditions.

VII. SIMULATION RESULTS UNDER NORMAL OPERATION CONDITIONS

Fig16. 3-Phase Instantaneous Active Reactive Power of MMC.

VIII. CONCLUSION

This paper presents the control methods of parallel-connected MMCs under both normal and switch fault-tolerant operation conditions. In order to reduce the calculation burden meanwhile increase the control accuracy of the internal circulating current suppression method; the resonant controllers are assumed in the synchronous reference frame to suppress the dominant second and fourth-order circulating current harmonics, and a sixth-order resonant controller is employed to suppress the zero-sequence internal circulating current. In addition, when the capacitor voltages are balanced as expected by using the voltage balancing control method, the external ZSCC can then be precisely controlled by treating the MMC as a simple two-level converter. This paper also proposes the fault-tolerant operation schemes as the switch in an SM suffers the open- or short-circuit failure. In principle, the fault-tolerant operation schemes will not influence the output quality by either adjusting the corresponding PWM schemes or the closed-loop control method. MATLAB simulations and the constructed experimental prototype verified the performance of proposed control method.

IX. REFERENCES


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