MDC FFT/IFFT Processor with Variable Length for MIMO-OFDM Systems

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Abstract: The architecture of multipath delay commutator (MDC) and memory scheduling are the basic concepts used to implement fast Fourier transform (FFT) processors with variable length. These FFT processors are used in orthogonal frequency division multiplexing systems, having multiple numbers of inputs and multiple numbers of outputs. Depending on this MDC architecture, we implement the FFT/IFFT processor based design which is proposed in this paper. In this design we implement ram, FIFO, input buffer and output sorting buffer. Based on the MDC architecture, we propose to use radix-N, butterflies at each stage, where Ns are the number of data streams, so that there is only one butterfly needed in each stage. Consequently, a 100% utilization rate in computational elements is achieved. This architecture can effectively reduce the silicon area necessary for the VLSI implementation of the Viterbi algorithm with the large constraint length. The existing system is a variable length FFT processor for MIMO-OFDM based SDR systems in which butterfly diagram is used in every stage of internal processing. So it will increase the processing time at result it will reduce the speed and take memory to store the each value in butterfly process. Finally it increases the memory size. It consists of only pipelined architectures.

A reduced memory FFT Processor can be implemented by using a Multi path delay commutator (MDC) based architecture. Only one MDC is used in the system and it will be available to every stage, so that the complexity and memory usage can be reduced. The MDC based system is efficient in terms of area but it is not efficient in terms of power. For the speed improvement we are proposing a new system with viterbi algorithm inside the FFT rather than the radix-2 algorithm. Furthermore, to apply the proposed scheme in practical applications, we let Ns = 4 and implement a 4-stream FFT/IFFT processor with variable length including 2048, 1024, 512, and 128 for MIMO-OFDM systems. This processor can be used in IEEE 802.16 Wi-MAX and 3GPP long term evolution applications. The processor was implemented with an UMC 90-nm CMOS technology with a core area of 3.1 mm². The power consumption at 40 MHz was 63.72/62.92/57.51/51.69 mW for 2048/1024/512/128-FFT, respectively in the post-layout simulation. Finally, we analyze the complexity and performance of the implemented processor and compare it with other processors. The results show advantages of the proposed scheme in terms of area and power consumption.

Keywords: Fast Fourier Transform (FFT), Memory Scheduling, Multiple-Input And Multiple-Output (MIMO), Orthogonal Frequency Division Multiplexing (OFDM), Output Sorting, Pipeline Based Multipath Delay Commutator (MDC), WiMAX.

I. INTRODUCTION

When we require a data to be encoded at multiple frequencies then the popular scheme generally used is orthogonal frequency division multiplexing. This type of scheme is famous at wideband digital communication. Whether it may be wired or wireless such as television, broadcasting of audio, internet accessing, wireless networks and is widely used in latest technology like 4G mobile communication. Digital multi carrier modulation technique is used for OFDM. When we require to carry parallel streaming of data, a large spaced orthogonal sub-carrier signals are used in which each sub-carrier undergo convolution modulation like quadrature amplitude modulation or phase shift keying. OFDM have capability of channel equalization because it uses slowly modulated narrow band signals instead of using one highly modulated wide band signal. Using OFDM, FFT can be implemented without loss in efficiency. Narrow band co-channel interfacing becomes very robust using OFDM it is very less sensitive over time synchronization errors. These types of OFDM signals have broad range of usage in WLAN under the standard of 802.11a, and digital radio systems standards like DAB/ERUKA 147, Terristial Digital TV systems (DVB-T) and Terrestrial Digital mobile systems (DVBT).

Fast Fourier transform are used to compute discrete Fourier transform and also for its inverse .These technique used to convert to signals from time to frequency domain and vice versa.fft makes numeric algorithm as simple such that it is used in image processing and signal processing applications. In previous DFT is existed, in which the fastness drawback has overcome by FFT.OFDM uses reverse FFT and transmitter side and FFT and the receiver side to perform modulation and demodulation efficiently. FFT with OFDM is used CPU like Intel Pentium at 1.26GHZ frequency and is able to calculate a 8 192 FFT...
with in 576\(\mu\)s using FFTW, and in CPU called intel Pentium M AT 1.6 GHZ frequency and able to within 387 \(\mu\)s. a compared to earlier generation CPU ,a wide range of FFT-OFDM based CPU named intel core 2 duo which operates at3 GHZ frequency and able to perform the operations at 96.

MIMO-OFDM defines multi input and multi output orthogonal frequency division multiplexing which is dominated over 4G and 5G wireless communications. The word multi input and multi output defines which is capable of sending multiple signals over multi antennas and orthogonal frequency division multiple communication system without loss in reliability. In earlier MIMO is used with a combination of time division multiple access, code division multiple access ,but MIMO with OFDM is much famous for its high data rate, high message deliver capacity ,high throughput .for these reasons only it is familiar at wires LAN and some standard networks at mobile communications . In MDC based MIMO OFDM as the data size increases the memory size also increases rapidly, but by using multipath delay commutator the data flow will be controlled in simplest manner the main reason for implementing MIMO based OFDM is for its simplicity and which makes the user data in to a closely spaced narrow sub channels in such to eliminates bigger obstacles to increase reliability.

In this case we propose a new pipelined architecture including viterbi algorithm within the FFT processor for moderate speed applications in wireless communications. There are several structural similarities between the FFT algorithm and viterbi algorithm. Their basic process element is a butterfly. The two number of application requirements such as: the size of the transform; the data word-lengths; the data word-widths; and the level of pipelining in the FFT processor. The transform size relates to the number of data samples in one data block, or data set, and is commonly expressed as the ‘point’ of the transform. Furthermore, algorithms have the same memory management and computation process. On the other hand, MDC schemes parse feedback paths into feed forward streams using switch-boxes with more memory. Meanwhile, the radix-\(r\) butterflies idle until the \(r\)th input is in position. Although the control of data flow in MDC is more straightforward, the utilization rate of the MDC FFT/IFFT computing core is \(1/r\), which is far less than the 100% utilization rate in SDF FFT/IFFT. Sansaloni et al. suggested that MDC could save more area than SDF in FFT with multiple streams, and Fu implemented a four-stream MDC FFT/IFFT processor in which the area was 75% that of conventional designs. To obtain parallelism, radix-2 butterflies were duplicated at the first stage. Together with storage elements, generally the first module occupied the largest area.

To the best of our knowledge, for the FFT/IFFT processors used in MIMO-OFDM systems, most of the researches intuitively duplicated the butterflies and memory according to the number of data streams, and then sought ways to maximize parallelism while reducing the hardware complexity. Also, few works have considered output memory needed for bit-reversed reordering for MIMO FFT/IFFT processors. These motivate us to explore FFT/IFFT architecture for MIMO systems, which can easily achieve a 100% utilization rate while the control mechanism is still simple. Meanwhile, we would like to reduce the memory requirement for managing bit-set-reversed output order in the new architecture. In this paper, we consider MIMO-OFDM systems with \(N\)s data streams, and propose to use single radix-\(N\)s butterfly at each folding stage to implement an MDC MIMO FFT/IFFT processor. In conventional radix-\(r\) MDC FFT/IFFT processor with single data stream, the utilization rate is \(1/r\). Hence, \((r-1)/r\) computing resource and memory are wasted. However, for a MIMO-OFDM system with \(N\)s data streams, if we let \(r = N\), the vacancy can be filled and thus the processor can achieve a 100% utilization. It is worthwhile to emphasize that by doing it we only need one butterfly at each pipeline stage.

Since we use one butterfly to process \(N\)s data streams at each pipeline stage, the input data need to be well scheduled before passing to the processor. Thanks to the simple control mechanism of MDC, we propose a simple mechanism for input scheduling, where the mechanism is scalable for \(N\)s being power of 2. Moreover, due to the use of one butterfly at each stage, we propose a simple output scheduling for bit/set-reversing, which can greatly reduce the required output memory. If the required output memory size is \(N\)s for single data stream, the size remains nearly \(N\)s\(r\) for multiple streams instead of \(N\)s\(r\) \(N\)s in conventional schemes, where multiple butterflies are needed in each pipeline stage. Furthermore, to apply the proposed schemes in practical applications, we let \(N\)s = 4 and implement a 4-stream FFT/IFFT processor with variable length including 2048, 1024, 512, and 128 as shown in Fig.1. This processor was implemented using an UMC 90 nm process and can be used in LTE or Wi-MAX applications.

The organization of this paper is as follows. Section II FFT/IFFT Processors .Section III FFT Processor Involved Methods .Section IV includes the hardware implementation, a synthesis report, and analysis of performance. Core area and power consumption are used to compare the proposed design with existing designs. Conclusions are provided in the last section.

$$\begin{align*}
128\text{-point decomposition:} & \quad \{4 \times 4 \times 8\} \\
512\text{-point decomposition:} & \quad 4 \times 4 \times 4 \times 8 \\
1024\text{-point decomposition:} & \quad 4 \times 4 \times 4 \times 4 \times 4 \\
2048\text{-point decomposition:} & \quad 4 \times 4 \times 4 \times 4 \times 8 \\
\end{align*}$$

Fig.1. Decomposition of four different FFT/IFFT lengths.
II. FFT/IFFT PROCESSORS

Fast Fourier Transform and Inverse Fast Fourier Transform are the most efficient and fast algorithms to calculate the Discrete Fourier Transform and Inverse Discrete Fourier Transform respectively. Fast Fourier Transform/Inverse Fast Fourier Transform is mostly used in many communication applications like Digital Signal Processing and the implementation of this is a growing research. From the last years, OFDM became an important one in FFT/IFFT algorithms and is going to be implemented. The efficient multiple access method for Bandwidth in digital communications is OFDM. Many of nowadays OFDM technique can be used in most important wireless communication systems: Digital Audio Broadcasting (DAB) (World DAB Forum, n.d.), Digital Video Broadcasting (DVB), Wireless Local Area Network (WLAN), Wireless Metropolitan Area Network (WMAN) and Multi Band –OFDM Ultra Wide Band (MB–OFDM UWB). Moreover, this method is also utilized in important wired applications like Asymmetric Digital Subscriber Line (adsl) or Power Line Communication.

Every communication system must have both Transmitter and Receiver. At the Transmitter side, IFFT is used for modulating signal, which depends on the OFDM system and at the Receiver side; FFT is used for demodulating signal. The FFT/IFFT is the important modules in OFDM transceivers. From this we can say that, the most parts of OFDM systems are, IFFT can be used at the transmitter side where as viterbi decoder can be used at the receiver side. The FFT is the second calculative huge block at the receiver section. The FFT and IFFT must be implemented such that to achieve the required throughput with the reduced area and delay as shown in Fig.2. The modern OFDM transceivers requirements may lead to the implementation of special hardware, which is the critical block in the transceiver. Hence the FFT/IFFT can be implemented as a Very Large Scale Integrated circuit. The methods that we applied to the FFT can also be applied to the IFFT. From the output of a FFT processor, we can easily get the IFFT. Therefore, the discussion in this chapter concentrates on the FFT without loss of generality.

The inverse discrete Fourier transform can be found using Which can be expressed as Where is called the twiddle factor We can see that the difference between the inverse discrete Fourier and forward Fourier transform is the twiddled factor and the division by 1/N is called the twiddled factor as shown in Fig.3.

Wireless technologies have evolved remarkably since Guglielmo Marconi said that the ability of radio can provide good contact with the ships sailing in the English Channel in 1894. New theories and applications of wireless technologies have been developed by hundreds and thousands of scientists and engineers through the world ever since. Wireless communications can be regarded as the most important development that has an extremely wide range of applications from TV remote control and cordless phones to cellular phones and satellite-based TV systems. It changed people's life style in every aspect. Especially during the last decade, the industry of mobile radio communication is growing exponentially with increasing rate, fueled by the digital and RF (radio frequency) circuits design, fabrication and integration techniques and more computing power in chips. This trend will continue with an even greater pace in the near future.

The advances and developments in the technique have partially helped to realize our dreams on fast and reliable communicating "any time anywhere". But we are expecting to have more experience in this wireless world such as wireless Internet surfing and interactive multimedia messaging so on. One natural question is: how can we put high-rate data streams over radio links to satisfy our needs? New wireless broadband access techniques are anticipated to answer this question. For example, the coming 3G (third generation) cellular technology can provide us with up to 2Mbps (bits per second) data service. But that still does not meet the data rate required by multimedia media communications like HDTV (high-definition television) and video conference. Recently MIMO-OFDM systems have
gained considerable attentions from the leading industry companies and the active academic community. A collection of problems including channel measurements and modeling, channel estimation, synchronization, IQ (in phase-quadrature) imbalance and PAPR (peak-to-average power ratio) have been widely studied by researchers. Clearly all the performance improvement and capacity increase are based on accurate channel state information. Channel estimation plays a significant role for MIMO-OFDM systems. For this reason, it is part of my dissertation to work on channel estimation of MIMO-OFDM systems.

Fig.4. Proposed MIMO FFT/IFFT Processor.

Multiple Input Multiple Output (MIMO) systems are devices that are used in wireless communication as shown in Fig.4. These are devices consisting of array of transmitters and receivers. With MIMO device it is possible to obtain high data. Hence combination of MIMO and OFDM system provides efficient data rate and reliability in wireless communications. IEEE 802.16 WiMAX (Worldwide Interoperability for Microwave Access) is a wireless communications standard, which can provide a data rates from 30 to 40 megabit/sec. 3GPP (3rd Generation Partnership Project) is the recent evaluation in IEEE 802.16 Wi-MAX. The 3rd Generation Partnership Project initiative evolved from a strategic one, which is between Nortel Networks and AT&T Wireless. AT&T Wireless was worked with an IS-136 time division multiple access wireless network present in the United States in 1998. Nortel Networks Wireless, which is an R&D center in Richardson, which is a wireless division of Bell Northern Research and developed a new one for “Internet Protocol” wireless network and the internal name is “Cell Web”.

III. FFT PROCESSOR INVOLVED METHODS

Fast Fourier Transform is an algorithm proposed by Cooley and Tukey to compute Discrete Fourier transform (DFT) which converts time to frequency and reduces the time complexity to O(N log 2N), where N denotes the size of FFT. When considering the other implementations, the FFT/IFFT algorithm is chosen such that the speed of execution, hardware complexity, flexibility and accuracy. But for real time systems, the speed of execution is the major thing. Based on this, Several architectures have been taken place from the last 300 years such as architecture having single and double memory, cached memory architecture, array based architecture, and pipeline based architecture for the purpose of hardware implementation, various FFT processors have been used mainly 2 types of architectures.

- Memory based architecture
- Pipeline based architecture

Memory based architecture cannot be parallelized where as the pipeline architecture can overcome the disadvantages of the former one. Pipeline based architectures worked in real time, continuous processing and having smaller latency with less delay which is required for most of the applications. Generally, the pipeline FFT processors are classified in two design architectures.

- Single-path delay feedback (SDF) pipeline architecture
- Multiple-path delay Commutator (MDC) pipeline architecture.

Single path delay feedback (SDF) reduces amount of multipliers but it complicates the control mechanism and uses more memory resources whereas Multipath Delay Commutator saves more area, and thus MDC is adopted as the hardware architecture. Multipath Delay Commutator (MDC) makes the feedback paths in to feed forward streams using switch boxes along with memory. In this paper Multipath Delay Commutator and memory scheduling are used to implement fast Fourier transform in orthogonal frequency division system with variable length for multiple inputs and multiple outputs. From the above two things, we can say that the delay feedback is more efficient than delay commutator for the proper utilization of memory. For computation of FFT we need to use twiddle factor to multiply with input signals to obtain output, and for this a huge size of ROM is required to store twiddle factors which in turn increases the cost. Thus for further improvement, ROM-less FFT/IFFT processor which eliminates ROM’s that store twiddle factor is presented. The complex multipliers are used for this purpose and they perform shift-and-add operations, thus the processor uses a digital multiplier with 2 inputs and does not require any storage element like ROM, to store twiddle factor. Thus the proposed architecture also includes a reconfigurable complex constant multiplier to store twiddle factor instead of using ROM”s.
IV. SIMULATION RESULTS

Simulation results of this paper is as shown in Figs.5 to 12.

Fig.5. 4-BIT FFT/IFFT.

Fig.6. 8-BIT FFT/IFFT.

Fig.7. 16-BIT FFT/IFFT.

Fig.8. 32-BIT FFT/IFFT.

Fig.9. 64-BIT FFT/IFFT.

Fig.10. 128-BIT FFT/IFFT.
The functionality of the proposed FFT/IFFT processor was implemented and verified by Xilinx 12.3 simulation. The circuit was synthesized by Synopsys Design Compiler using an UMC 90-nm CMOS cell library. The system clock for synthesis was targeted at 40 MHz. It is worth pointing out that one of the advantages using pipeline architecture is the reduction of critical path. Pipeline registers were inserted at all outputs of memory macros, multipliers, and radix-4 and radix-8 butterflies. In fact, we found the maximum achievable clock rate of the proposed design can be as high as 250 MHz in synthesis stage.

The power consumption was analyzed primarily by Synopsys Prime Power with the net-list extracted from actual APR. We also use the power analysis function in SoC Encounter. The measured results using these two tools only have a small mismatch within 5 mW. Fig.13 lists the pie diagram of area and power consumption. Excluding the testing function, the memory occupied 85.95% of the total area. The ratio of standard cells versus SDRAM macros was close to 1/5. This means if more advanced (that is, high density) memory macros were applied, further reduction could be achieved. The power consumption at 40 MHz system clock were 63.72 mW for 2048-FFT, 62.92 mW for 1024-FFT, 57.51 mW for 512-FFT, and 51.69 mW for 128-FFT computations.

**B. Performance Analysis and Comparison**

Throughput, signal to noise quantization ratio, and normalized area/power consumption are the major indices used to evaluate the performance of FFT/IFFT processors. Let us compare the proposed design with other existing designs. Most of the previous works were based on SDF or memory base radix-2² algorithm. Bass proposed methods to
evaluate the normalized area $A_{\text{bass}}$ and normalized power consumption $P_{\text{bass}}$ among different kinds of FFT processor as follows:

$$A_{\text{bass}} = \frac{\text{Area}}{(\text{Tech}/0.5\,\mu\text{m})^2} \quad (1)$$

$$P_{\text{bass}} = \frac{\text{Tech} \times (\frac{\text{Width}}{8} + \frac{\text{Width}}{3})}{\text{Power} \times \text{Exec Time} \times 10^{-6}} \quad (2)$$

Where Tech is the process in micrometers, Width is the bit width of data-path in bits, and Exec Time is the calculation time in microseconds. Baas’s comparisons were used for FFT/IFFT designs that have the same N, and similar architecture with coarse adjustment corresponds to different CMOS process. In addition to the architecture, different FFT length N, system frequency, and applied CMOS processes fundamentally affect the area and power consumption. Thus Peng considered different FFT/IFFT length N and proposed the normalized area $A_{\text{peng}}$ and normalized power $P_{\text{peng}}$ as

$$A_{\text{peng}} = \frac{\text{Area}}{N \times (\text{Tech}/0.18)^2} \quad (3)$$

$$P_{\text{peng}} = \frac{\text{Power} \times \text{Exec Time}}{N \times (V_{\text{DD}}/1.8)^2} \quad (4)$$

Now let us consider a more general evaluation as follows. The computational complexity for an N-point FFT/IFFT in radix-r is $N \log_r N$ [8]. In practical implementation, the addition and multiplication operations can be well scheduled and executed by a small number of radix-r butterflies and complex multipliers. In such a case, the complexity of different N-FFT/IFFT should grow in logarithmic scale instead of linear scale. As for different radix-r butterflies, the implementations are still based on fundamental radix-2 structure. When N increases, the number of pipeline stages is proportional to $\log_2 N$. Therefore, the comparison should be normalized to the fundamental radix-2 structure. The power consumption is proportional to load capacitance, supply voltage, and operating frequency, that is, $P \propto CV^2F$. For comprehensive and comparable analysis among various N, architecture, technology and number M of data streams, we may revise the area metric as

$$A_{\text{propose}} = \frac{\text{Area} \times 10^3}{(\text{Tech}/0.09\,\mu\text{m})^2 \times M \times \log_2 N} \quad (5)$$

and the metric for power consumption as

$$P_{\text{propose}} = \frac{\text{Power} \times \text{Exec Time} \times 10^8}{M \times V_{\text{DD}}^2 \times N \log_2 N} \quad (6)$$

Note that the $V_{\text{DD}}$ in 0.09 μm process is 1 volt. There are still other factors that affect the comparing criterion, such as the type of applied RAM macros, the overall load capacitance, or different synthesis constraints. Meanwhile, the factor of system frequency is not included in the revised metrics. Generally different operating frequencies in similar design lead to different synthesis and APR results.

Table II compares the proposed scheme and other works. As previously stated, different fabrication technology and synthesis constraint affect the basis in comparison. Therefore, the FFT/IFFT processors with the same N are grouped for discussion. For FFT/IFFT processors with N = 128, the normalized area for the MDC scheme is 67% ~ 77% of that for SDF schemes. Note that with higher clock rate, the normalized energy is reduced at the cost of larger normalized area. The trend can be carried on to 512-and 2048-FFT/IFFT processors as that. Now consider the FFT/IFFT processors with a large size of N = 2048, where memory macros and storage elements dominate.
the die area. Although the normalized area in the memory base processor is smaller, the normalized energy is not reduced proportionally. This is because the memory-based scheme uses twice amount of memory than those in pipeline schemes with continuous output. As long as the memories are accessed by computing elements, the macros consume power. Consequently, to effectively reduce the area and power consumption in large N-FFT/IFFT processor, decreasing memory usage may be a key solution. Moreover, the output latency of the memory-based FFT/IFFT processors can be as long as one OFDM symbol. Thus it is not able to handle successive OFDM symbols unless extremely high clock is used to handle relatively slow data.

Trying to seek a good trade-off between these conventional schemes, the proposed FFT/IFFT processor adopts simple memory scheduling methods for both input and output data; this enables the processor to use a relatively small amount of memory to handle successive and multiple data streams. Observed from Fig.13, the memory part, which includes input memories, intermediate FIFOs, and output sorting, takes 85.95% of the overall area and 61.72% of the overall power consumption. As a result, the scheduling methods not only reduce the area but also contribute to power saving. Comparing with, the proposed FFT/IFFT processor uses fewer computing elements, and the execution time is only one forth of that for main distribution frame (MDF) scheme. Moreover, due to the use of output memory scheduling, the proposed FFT/IFFT processor can handle four data streams and produce bit/set-reversed output data simultaneously, from integration perspective, the adjacent functional blocks such as frequency domain equalizer can directly apply the bit/set reversed results from FFT/IFFT processor without additional effort for reordering.

Fig.14 converts the execute time per symbol into the throughput in terms of k-symbol per second. The corresponding clock rate, normalized power and area are also marked to show the design trade-off. Although the FFT/IFFT processor is of the highest throughput with the minimal normalized energy, it is at the cost of the largest normalized area and the maximal operational rate at 300 MHz. Note that the FFT was specifically for 16 quadrature amplitude modulation application and the word-size for real part and imaginary part is only 4-bit. Among the 2048-point FFT/IFFT processors with clock rate below 50 MHz, our proposed design is of the highest throughput.

V. CONCLUSION

The proposed high speed MDC architecture and memory scheduling are very much suitable for FFT/IFFT processor in multiple input multiple output OFDM system, because the constant multipliers are used to store the twiddle factors instead of ROM, Which utilizes 100% area and reduces the delay. The new algorithm proposed a radix-r based MDC MIMO FFT/IFFT processor for processing Ns streams of parallel inputs, where r = Ns for achieving a 100% utilization rate. The proposed approach is suitable for MIMO-OFDM baseband processor such as WiMAX or LTE applications. We proposed an efficient memory scheduling to fully utilize memory. This considerably decreases the chip area because the memory requirement usually dominates the chip area in an FFT/IFFT processor. However, by using the proposed memory scheduling, MDC architecture is proved suitable for FFT/IFFT processors in MIMO-OFDM systems, because the butterflies and multipliers are capable of achieving a 100% utilization rate, meanwhile, the characteristics of simple control provided by MDC is maintained in the proposed design. The reduction in memory usage also leads to effective power saving, which is important for mobile devices. For applications applying large number N, of data streams such as gigabit passive optical network, N can be as high as 64. In this case, the proposed radix-N, MDC scheme and memory scheduling may also be applied to achieve a 100% utilization rate with simple control mechanism. Therefore, we conclude that the proposed designs found a good balance among complexity, energy consumption, and chip area, for the MIMO-OFDM systems.

VI. REFERENCES

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