A TRI-Loop Full-Spectrum Power Supply Rejection Low-Dropout Regulator

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Abstract: High performance low-dropout regulator (LDOs) are indispensable in a system on-a-chip (SOC) due to their low output noise, fast transient response and good power supply rejection (PSR) characteristics. It is proposed to provide a clean supply for noise-sensitive buildings blocks in wideband communication systems. The LDO is implemented in 90nm CMOS technology and achieves a PSRR better than -19.15dB@1GHz for load currents up to 100mA. The Voltage Regulator provides maximum 10mA Current, moreover with a 1.2V supply voltage, this LDO regulator providing an output of 1V with a 200mV dropout voltage.

Keywords: 90nm Technology, Flipped Voltage Follower, Low-Dropout Regulator (LDO), Power Supply Rejection (PSR).

I. INTRODUCTION

Switch Mode power converters in power management units generate high levels of switching noise. A linear regulator can filter out the noise and provide a clean supply voltage to drive noise-sensitive circuits such as trans-impedance amplifiers (TIA) or low-noise amplifiers (LNA) in wireline and/or wireless communication front-end systems [1], [2], as well as critical paths in VLSI chips [3]. Therefore, high performance low dropout regulators, commonly known as LDOs, are indispensable in a system-on-a-chip (SoC) due to their ripple free, fast transient response and good power supply rejection (PSR) characteristics.

In general, differential analog circuit loads need an LDO with high PSR; digital circuit loads need an LDO with fast load transient response [3]; while single-ended analog/RF circuit loads need an LDO with both high PSR and fast line and load transient responses [2]. Off-chip LDOs or on-chip LDOs with off-chip decoupling capacitors are commonly used for rejecting supply noise. However, an off-chip capacitor cannot effectively reduce the supply noise at the point-of-load, due to the bond-wire effect. Thus, fully-integrated area-efficient LDOs are highly desirable for point-of-load power delivery and multi-voltage systems [4]. In addition, supplying power to individual noise-sensitive and/or noise-generating building blocks with separate LDOs can improve the system performance considerably. Fig 1 shows an LDO embedded in an optical receiver that helps improving the front-end sensitivity [5], [6].

Fig. 1. An optical receiver with embedded LDO.

The single-ended (or pseudo-differential) TIA has only one photodetector, and supply variations would degrade its sensitivity severely [2]. The data rate of an optical receiver could be over 10 Gb/s, the digital output buffer and/or clock and data recovery circuits will generate GHz on-chip noises, thus, the LDO needs to have PSR for the frequency range from DC to 20 GHz in such system. With a large off-chip output capacitor, say 1 , small ripples due to load transients can be achieved and bandwidth can be extended using techniques such as load-current dependent boost current [7], dynamically-biased buffer impedance attenuation (BIA) [8], adaptively-biased super current mirror [9], and multiple small-gain stages in nanometer processes [10]; while high PSR can be achieved using feed-forward ripple cancellation techniques [11]. However, for fully-integrated LDOs, large load capacitors are no longer available, and both transient response and PSR will degrade significantly. Small form factor and low cost are the driving factors for full integration. Many fully-integrated LDOs with limited on-chip capacitance (a.k.a. capacitorless LDOs) have been proposed in the past decade [12]–[19]. To make a comparison, a figure-of-merit (FOM) of LDOs is defined in [13] and widely adopted by other researchers. It reads

\[ FOM = \frac{T_h}{I_{Q}} \times \frac{I_{Q}}{I_{Q}} \times \frac{\Delta V_{OUT}}{V_{IN} - V_{OUT}} \times \frac{C}{V_{IN} - V_{OUT}} \]

where is the quiescent current, and the response time is a function of the total on-chip capacitance , load-transient glitches of the output voltage and the maximum load current. To achieve full integration, some specifications have to be sacrificed.

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Fig.2. Magnitude plot of a generic LDO with two low frequency poles: (a) with being its dominant pole; and (b) with being its dominant pole.

Table I. LDO Categorization by Dominant Pole Location

<table>
<thead>
<tr>
<th>Integration</th>
<th>With Off-Chip Cap.</th>
<th>Fully On-Chip</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dominant pole</td>
<td>$P_{Gate}$</td>
<td>$P_{Out}$</td>
</tr>
<tr>
<td>Process Scaling</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Limit on $I_{Q_{min}}$</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>UGF</td>
<td>–</td>
<td>$V$</td>
</tr>
<tr>
<td>Transient $\Delta V_{Out}$</td>
<td>–</td>
<td>$V$</td>
</tr>
<tr>
<td>PSR</td>
<td>$V$</td>
<td>$V$</td>
</tr>
<tr>
<td>$I_{Q}$</td>
<td>$V$</td>
<td>–</td>
</tr>
</tbody>
</table>

In [13], a folded cascode stage was used to increase the DC gain, and a considerably large current (6%) was used to move the non-dominant poles to high frequencies, resulting in a mediocre current efficiency of 94%. A cascode structure with 600 mV dropout voltage was employed in [14] that significantly improved the PSR performance, but also considerably degraded the transient response. A single transistor control LDO based on the flipped voltage follower (FVF) topology, which is the simplest FVF architecture, provided stable voltage regulation for a wide range of output capacitor values including the output capacitor-less case in [15], but it was sensitive to process, voltage and temperature (PVT) variations, and was not fast enough with 160 mV load-transient undershoots observed. The FVF with folded cascode stage was also employed in [16] with slew-rate enhancement circuit that responded to 100 ns load-transient edges; however, its PSR degraded to 0 dB before reaching 1 MHz. An ultra-fast response comparator-based regulator in 45 nm SOI process was proposed in [17] that consumed 12 mA of quiescent current and required an on-chip deep-trench capacitor of 1.46 nF, and its intrinsic 10 mV ripple is not suitable for supplying the RF/analog front-end systems. [25] was using a non-inverting gain stage for higher loop gain and Miller compensation for stability, but only provides simulations results with 100 ns edge times.

From the literature review above, we conclude that there is a gap between the performances of fully-integrated and nonfully-integrated LDOs. An area-efficient LDO with ultra-fast response and full spectrum PSR is in high demand. In this research, a tri-loop LDO is proposed that achieves an FOM of 5.74 ps and PSR of better than 12 dB over the whole spectrum (DC to 20 GHz tested). The basic idea of this design is to take advantage of the advanced processes by keeping most of the limited available capacitance at the output node for better PSR and transient response, and pushing the internal poles to be higher than the unity-gain frequency (UGF) by using buffer impedance attenuation (BIA) and flipped voltage follower (FVF) techniques. Consequently, the performance is improved with process scaling. In the proposed tri-loop architecture, the BIA technique is integrated into the FVF structure with the output node being the dominant pole, and a tri-input error amplifier (EA) is proposed to improve the DC accuracy. This paper is organized as follows. Considerations of the proposed architecture and the existing circuit techniques are discussed in Section II. Circuit implementation, stability and PSR analyses of the proposed tri-loop LDO are discussed in Section III. Measurement results of the prototype tri-loop LDO are presented in Section IV, followed by conclusions in Section V.

II. ARCHITECTURAL CONSIDERATIONS

A. Dominant Pole Considerations

For an LDO, the largest capacitors are the output filtering capacitor $C_{L}$ and the parasitic gate capacitor $C_{g}$ of the power MOS transistor. Hence, there are at least two low-frequency (LF) poles on the left-half-plane (LHP): the pole at the output node, and the pole at the gate of the power MOS $P_{Gate}$, as sketched in Fig2 with either or being the dominant pole. The pole would shift to a lower frequency when the load resistance increases and vice versa. Basically, LDOs with an off-chip filtering capacitor are designed to be dominant [7], [9]–[11], while all fully-integrated analog "capacitor-less" LDOs have an internal dominant pole $P_{Gate}$ [12]–[16], [18], [19]. Thus, LDOs can be classified by the need for an off-chip capacitor or not, or they can be classified by being output-pole dominant or internal-pole dominant. Therefore, there are 4 combinations of which the pros and cons are summarized in Table I and discussed as follows. There are many benefits in designing as the dominant pole by using most of the available capacitance at the output node. First of all, a larger output capacitor filters out power supply noise and glitches and serves as a buffer for load-transient current changes, resulting in a smaller $\Delta V_{Out}$. Second, as discussed in [20], because the output voltage is well regulated by the control loop at low frequency, and the noise is bypassed to ground by high frequency, the worst case PSR would occur at medium frequency. Thus, increasing both the output capacitance and the loop bandwidth (that is, the unity-gain frequency UGF) would improve the PSR. Third, moves to lower and lower frequency as the load current decreases, which is better for the loop stability comparing to the internal-pole dominant case. In fact, the zero-load condition is not even discussed in many output-capacitor-less designs, and instead, a minimum load current is needed to satisfy stability requirements. If is reduced to satisfy stability requirements, the high frequency PSR performance will be degraded, and is not acceptable in our application. For the dominant case, pole-zero cancellation is usually used to extend the loop bandwidth and to enhance the stability.

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International Journal of Advanced Technology and Innovative Research
Volume. 09, IssueNo.10, September-2017, Pages: 1695-1698
The LHP zero may be generated by the equivalent series resistance (ESR) of \( C_{\text{L,OR}} \) by a high-pass feedback network as proposed in [12]. Alternatively, the non-dominant pole may be pushed to frequencies higher than the UGF by circuit techniques mentioned in [7]–[10]. The only drawback with the dominant case is that a relatively high quiescent current is needed to push the internal poles to higher frequencies. This requirement can be relaxed by using advanced processes that have lower parasitic capacitance. The transistors will have smaller feature sizes, and the internal poles could be moved to higher frequencies with the same bias current. At the same time, smaller can be used and results in smaller chip area and higher UGF. To summarize, an LDO being dominant can benefit from the process scaling that is one of the most desirable characteristics in integrated-circuit design. The proposed architecture will be introduced in Section III.

B. Flipped Voltage Follower

The replica biasing technique is widely used in source-follower based or flipped-voltage-follower (FVF) based LDOs for supplying power to digital ICs with ultra-fast load-transient responses. The schematic of a single-transistor-control LDO based on FVF it is shown in Fig. 3 as an example. This circuit can be divided into three parts: the error amplifier (EA), \( V_{\text{SET}} \) the generation and the flipped voltage follower. For simplicity, we assume \( I_1 = I_2 \) and \( (W/L)_1 = (W/L)_2 \). The mirrored voltage \( V_{\text{Mir}} \) is controlled to be equal to \( V_{\text{REF}} \) by the EA, and is generated from by the diode-connected \( M_2 \). Followed by a FVF, \( V_{\text{OUT}} \) is set by \( V_{\text{SET}} \) through \( M_8 \), and it is a mirrored voltage of \( V_{\text{Mir}} \). In the FVF, \( M_8 \) act as a common-gate amplifying stage from \( V_{\text{OUT}} \) to \( V_G \). Obviously, there are two low-frequency poles \( (p_{\text{Gate}} \) and \( p_{\text{Out}} \)) in the FVF when a relatively large on-chip \( C_L \) (ranging from 100 pF to 1 nF) is used to handle the load current that ranges from 0 to 10 mA. This topology is very difficult (if not impossible) to be stable if \( p_{\text{Out}} \) is the dominant pole. In \( p_{\text{Gate}} \) dominant, it is adopted using a small \( C_f \) (or even no \( C_f \)). In, \( p_{\text{Gate}} \) dominant is also adopted with an ESR zero; adaptive voltage positioning by intentionally setting \( V_{\text{OUT}} \) to a lower value at heavy load was used. However, lower \( V_{\text{OUT}} \) is undesirable for analog loads.

Another issue associated with this structure is the DC accuracy of \( V_{\text{OUT}} \).

The offset voltage between \( V_{\text{REF}} \) and \( V_{\text{OUT}} \) can be divided into two parts. First, there is an offset between \( V_{\text{REF}} \) and \( V_{\text{Mir}} \) that consists of systematic and random offsets of the EA. Second, the mismatches between the voltage mirror (\( M_7 \) and \( M_8 \)) and the bias currents (\( I_1 \)and \( I_2 \)) will generate an offset between \( V_{\text{Mir}} \) and \( V_{\text{OUT}} \). Hence, the FVF-based topology has low immunity to PVT variations. Moreover, the loop gain of the FVF is low, which results in poor load regulation. Nevertheless, due to its potential for fast transient response and low voltage characteristics, the FVF structure is used as the starting point, and improvements will be discussed in Section III.

C. Buffer Impedance Attenuation

To realize the LDO with \( p_{\text{Out}} \) dominant, \( p_{\text{Gate}} \) in Fig. 3 should be pushed to high frequency not only by using large bias current \( I_2 \) but also with additional circuitry. A buffer can be inserted between the gain stage with high output impedance and the power stage with large input capacitance [9], as shown in Fig. 4. The buffer presents low input capacitance to \( V_A \) and low output impedance to \( V_G \), pushing the two poles at \( p_A \) and \( p_{\text{Gate}} \) to high frequencies. In this design, the output capacitor \( C_L \) is 130 pF, the bias current \( I_2 \) is 20 µA, and the buffer consumes another 20 µA at light load (60 µA at heavy load), and all the above help pushing \( p_{\text{Gate}} \) to the GHz range. The remaining problem is the low DC accuracy of \( V_{\text{OUT}} \).

III. PROPOSED TRI-LOOP LOW-DROPOUT REGULATOR

In this research, a fully-integrated tri-loop low-dropout regulator designed in a 65 nm CMOS general purpose (GP) process is proposed to achieve ultra-fast transient response and full spectrum (DC to 20 GHz tested) power supply rejection with limited chip area, current budget and voltage headroom. The transistor-level schematic is shown in Fig. 5.

A. Tri-Loop Architecture

To increase the DC accuracy of the FVF-based LDO, a third loop is introduced through using a tri-input EA. In previous architectures, only \( V_{\text{Mir}} \) is fed forward to generate \( V_{\text{OUT}} \), and \( V_{\text{OUT}} \) is not fed back to the EA. Now, the EA
compares $V_{\text{REF}}$ with both $V_{\text{MIR}}$ and $V_{\text{OUT}}$, and the W/L ratios of the three input transistors $M_1$, $M_2$, and $M_3$ are $(W/M)_1 : (W/M)_2 : (W/M)_3 = 4:1:3$ such that $V_{\text{OUT}}$ is computed to be

$$V_{\text{OUT}} = \frac{A_{\text{EA}}}{1 + A_{\text{EA}}} V_{\text{REF}} - \frac{\Delta V A_{\text{EA}}/4}{1 + A_{\text{EA}}} \approx V_{\text{REF}} - \frac{\Delta V}{4}$$

where $A_{\text{EA}}$ is the gain of the EA (including the $V_{\text{SET}}$ generation stage), and $\Delta V$ is the voltage difference between $V_{\text{MIR}}$ and $V_{\text{OUT}}$ due to PVT and load variations. By substituting (3) into (2), and assuming $A_{\text{EA}} >> 1$, we have

$$V_{\text{OUT}} = \frac{A_{\text{EA}}}{1 + A_{\text{EA}}} V_{\text{REF}} - \frac{\Delta V A_{\text{EA}}/4}{1 + A_{\text{EA}}} \approx V_{\text{REF}} - \frac{\Delta V}{4}$$

Therefore, is closer to than by setting the size ratio of and to be 1:3.

**B. Circuit Implementation**

Since the EA is not in the high-speed path, the input transistors of the EA and its tail current mirror are implemented with 2.5-V I/O devices for DC gain and ESD considerations. Different symbols are used to distinguish the I/O devices from the 1-V core devices in Fig. 5. All on-chip MOS capacitors are I/O devices to avoid gate leakage current if thin-oxide (1.0 V) devices are used. Transistors in the FVF stage are all thin-oxide devices for fast response. To suppress off-chip noise, a 2 pF $C_{\text{IB}}$ is added at the bias input node $I_{\text{bias}}$, and may not be needed if $I_{\text{bias}}$ is generated on-chip. To save static current, the ratio of $M_7$ and $M_8$, and that of their bias currents, is set to be 1:4, as $V_{\text{SET}}$ is in the low-speed path that does not need much current, but $V_A$ is in the high-speed path and needs more current. The buffer used for impedance attenuation consists of $M_9$ through $M_{13}$, and three parameters are of concern: the input capacitance $C_{\text{IB}}$, the output resistance $r_{\text{OB}}$, and the DC gain $A_B$. The small-signal model of the buffer is shown in Fig. 6. The input capacitance of the circuit can be computed by noting that

$$C_{\text{IB}} V_{\text{gB}} = C_{\text{gs}} V_{\text{gs}} + C_{\text{gd}} V_{\text{gd}}$$

and in the small-signal limit, (6) can be rewritten as

$$C_{\text{IB}} = \left(1 - v_s/v_B\right) C_{\text{gs}} + \left(1 - v_d/v_B\right) C_{\text{gd}}$$

where $C_{\text{gs}}$ and $C_{\text{gd}}$ are the gate-to-source and gate-to-drain capacitances of $M_9$. The voltage gains are calculated as

$$A_B = \frac{v_d}{v_s} = \frac{1}{(1 + A_1 A_2) A_1 A_2}$$

with

$$A_1 = \frac{g_m}{g_{ds}}$$

and

$$A_2 = \frac{(8 g_{m11} + 8 g_{d11})}{g_{dsr}}$$

$$g_{dsr} = g_{m10} + g_{ds10} + g_{ds11} + g_{ds13}$$

and

$$\frac{v_d}{v_s} = \frac{-v_d}{-v_s} = -\frac{A_1}{A_1 A_2}$$

Here, $A_1$ is the intrinsic gain of $M_9$, and $A_2$ is the gain from the drain to the source of $M_9$. Assume $A_1$ and $A_2$ to be much larger than 1, then $A_B \approx 1$. Combining (7), (8), and (12), we have

$$C_{\text{IB}} = \frac{A_2 + 2}{A_1 A_2 + A_2 + 2} C_{\text{gs}} + \left(1 + \frac{A_1}{A_1 A_2 + A_2 + 2}\right) C_{\text{gd}} \approx \frac{1}{A_1} C_{\text{gs}} + \left(1 + \frac{1}{A_2}\right) C_{\text{gd}} \approx C_{\text{gd}}$$

Since $M_9$ operates in the saturation region, most of the channel charge is associated with the source, which means that $C_{\text{gs}}$ is much larger than $C_{\text{gd}}$, and hence, $C_{\text{IB}}$ is small. The output resistance of the buffer $r_{\text{OB}}$ is given by
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\[
\text{r}_{\text{out}} = \frac{1}{A_3(g_{m10} + g_{d10}) + g_{m10} R_T}
\]

(14)

where \( A_3 = (g_{m11} + g_{d11})/(g_{d12} + g_{d10}) \). This gain needs to be increased to further attenuate \( r_{\text{out}} \). Note that \( g_{d10} \) includes the term \( g_{m10} \) from \( M_{10} \), and lowering \( r_{\text{out}} \) by increasing \( g_{m10} \) also increases the pull-up capability of the buffer.

A fundamental design trade-off is identified between the DC gain and the frequency response: to satisfy the assumption that \( A_1, A_2 >> 1 \), the channel length \( L \) of \( M_0 \) should be long for \( A_1 >> 1 \), and the \( L \) of \( M_{11} \) should be long for \( A_2 >> 1 \); to reduce \( C_{gs} \) and \( C_{gb} \), \( L \) of \( M_0 \) and \( M_{11} \) should be short. In this design, the minimum \( L \) is used for \( M_0 \) and \( M_{11} \) for speed consideration, and \( M_{11} \) operates in the sub- or near-threshold region (in light or full load conditions, respectively) to give a larger \( g_{m11} \) to increase \( A_1 \) and \( A_2 \). The gate capacitance of \( M_{11} \), which would generate an additional pole \( p_0 \) at node \( V_D \), is neglected in the analyses above. This non-dominant pole \( p_0 \) is located in the GHz range as verified by the following AC simulations and transient measurement.

C. Stability Analyses

The signal paths of each loop are superimposed on the schematic shown in Fig.7. Each loop has a different function: Loop-1 is an ultra-fast low-gain loop with \( p_{\text{out}} \) being its dominant pole, and non-dominant poles \( p_{\text{Gate}} \) and \( p_A \) are pushed to the GHz range by the buffer impedance attenuation technique; Loop-2 is composed of the EA and the diode-connected \( M_1 \) and is a slow loop that generates the voltages of \( V_{\text{mir}} \) and \( V_{\text{SET}} \); Loop-3 has \( V_{\text{OUT}} \) fed back to the EA such that the DC accuracy is improved. In other words, Loop-1 is used to deal with the fast load-transient current, while Loop-3 is used to enhance the \( V_{\text{OUT}} \) DC accuracy. To simulate the loop response of each loop, three simulation setups are configured and described as follows.

Setup 1: As shown in Fig. 8, the signal path of Loop-1 is broken between \( V_A \) and the buffer input. The AC small signal is injected to the buffer input and the output is observed at \( V_A \). To isolate the influence from Loop-2 and Loop-3, the path from \( M_2 \) to \( M_8 \) is also broken. To maintain the DC bias point, a DC voltage \( V_{\text{SET}} \) is applied to the gate of \( M_8 \). And to account for the loading effect, a replica buffer stage is added to \( V_A \) to mimic \( C_{iB} \).

Setup 2: Loop-2 and Loop-3 are broken from \( V_{\text{mir}} \) to \( M_2 \) and from \( V_{\text{OUT}} \) to \( M_3 \), respectively, as shown in Fig. 9. The AC small signal is injected into the EA through \( M_2 \) only. Now, the AC response of Loop-2 can be obtained at \( V_{\text{mir}} \), and the response of Loop-3 can be obtained at \( V_{\text{OUT}} \), simultaneously.

Fig.8. Break Loop-1 with replica buffer to mimic its input capacitance.

Fig.9. Break Loop-2 and Loop-3 simultaneously for stability analysis.

Loop-2 and Loop-3 can be considered together because they both contain the error amplifier in their respective loops. Simulation results of these two setups are combined in Fig.10, which shows the Bode plots of the three loops at heavy load condition with \( R_L = 100\Omega \). When \( V_{\text{OUT}} \) is 1.0 V, Loop-1 has a DC gain of 21 dB and its UGF is 600 MHz, with a phase margin (PM) of 60°. Loop-2 has one dominant pole located at \( V_{\text{SET}} \) and a non-dominant pole located at \( V_{\text{EA}} \), and PM2 = 80°. Loop-3 has two non-dominant poles located at \( V_{\text{OUT}} \) and \( V_{\text{EA}} \), respectively, and PM3 is only 20°. Nevertheless, the stability of the circuit is determined by the system loop gain, not individual loop gains. A third loop-breaking setup for stability analysis is shown in Fig. 11, and described as follows.

Setup 3: Loop-2 and Loop-3 contain the error amplifier, and by breaking the loops between \( V_{\text{EA}} \) and the gate of \( M_6 \) we have

\[
V_{\text{CA}} = \frac{g_{m2}(r_{o1}\|r_{o4})}{1+sC_{\text{EA}}(r_{o1}\|r_{o4})}(V_{\text{mir}}+3V_{\text{OUT}})
\]

(15)

\[
\frac{V_{\text{mir}}}{V_{\text{SC}}} \approx \frac{-g_{m6}(r_{o6}\|r_{o15})}{1+sC_{\text{GB}}(r_{o6}\|r_{o15})}
\]

(16)

\[
\frac{V_{\text{OUT}}}{V_{\text{mir}}} \approx \frac{1}{1+1/A_7(s)}
\]

(17)

\[
\frac{V_{\text{SET}}}{V_{\text{mir}}} \approx \frac{1}{1+1/A_7(s)}
\]

(18)
Fig. 10. Simulated frequency response of the three loops of the proposed LDO with $V_{IN} = 1.2V$, $V_{OUT} = 1.0V$, and $R_L = 100\Omega$.

Fig. 11. Break the loop at the EA output.

with

$$A_7(s) = \frac{8mT_{a15}}{(1 + sC_{B1}R_{a15})} \tag{19}$$

$$A_B = \frac{g_{m8}r_{o8}}{1 + sC_{EA}r_{o8}} \tag{20}$$

$$A_P(s) = \frac{8mT_{a2}(R_{L})}{1 + sC_{L}(R_{OP})(R_{L})} \tag{21}$$

$$T(s) = \frac{v_{ac}}{v_{ac}} = \frac{g_{m2}(r_{o2})(r_{o3})(1 + sC_{EA}(r_{o1})}(1 + sC_{B1}(r_{o1}))}$$

$$+ \frac{g_{m2}(r_{o2})(r_{o3})(1 + sC_{EA}(r_{o1}))}{1 + sC_{B1}(r_{o1})(r_{o3})(1 + sC_{B1}(r_{o1})(r_{o3}))} + \frac{A_7(s)}{A_7(s)}$$

$$\approx \frac{(1 + sC_{B1}(r_{o1}))}{(1 + sC_{EA}(r_{o1}))} \frac{1 + A_7(s)}{1 + A_7(s)} \approx \frac{g_{m2}(r_{o2})(r_{o3})(1 + sC_{B1}(r_{o1})(r_{o3}))}{1 + sC_{B1}(r_{o1})(r_{o3})(1 + sC_{B1}(r_{o1})(r_{o3}))} \tag{22}$$

where $v_{ac}$ is the AC signal injected at the gate of $M_6$, $C_{EA}$ is the parasitic capacitance at the $V_{EA}$ node, and $r_{o8}$ is the output resistance of $M_{max}$. The loop-gain transfer function of the entire LDO is given by (22), at the bottom of the page. There are three LHP poles and one LHP zero in the transfer function, while the dominant pole is generated by $C_B$. The zero is generated by Loop-2, which is a shorter path compared to Loop-3. It is a pole-zero tracking pair that makes the entire LDO stable in all loading conditions. The simulated Bode plots of Setup 3 in different corners are given in Fig. 12. The worst case phase margins are $68^\circ$ at 10 mA loading ($R_L = 100\Omega$) and $38^\circ$ at no load condition, respectively.

Fig. 12. Simulated Bode plot of the LDO with $V_{IN} = 1.2V$, $V_{OUT} = 1.0V$ and, at the corners of TT at $25^\circ$, SS at $85^\circ$ and FF at $-20^\circ$.

In this research, the (W/L) ratio of $M_2$ and $M_3$ is aggressively set to be 1:3. This setting is to trade stability margin for better $V_{OUT}$ DC accuracy. To gain more design margin for stability, the weighting of $M_2$ and $M_3$ could be set to 2:2 by satisfying with lower DC accuracy. Alternatively, in another extreme case, with $M_2$ (Loop-2) being removed and $M_3$ having the same size as $M_1$, the DC accuracy is maximized. However, the dominant pole of Loop-3 at $V_{SET}$ has to be much lower than before, and the settling time of $V_{OUT}$ will be much longer due to slow Loop-3.

D. Load Regulation

Curves of load regulation are shown in Fig. 13, with (W/L)$_2$: (W/L)$_3$ being set to 1:3, 2:2, and 1:0 (no Loop-3) respectively. In the case of no Loop-3, $V_{OUT}$ changed by 34 mV when the load current is changed from 10μA to 10 mA. For our proposed case of 1:3, $V_{OUT}$ changed by only 11 mV with the same change in load current. DC accuracy is improved by about 3 times by adding Loop-3 without degradation in stability and speed performance. If the ratio of $M_2$ and $M_3$ is 2:2, $V_{OUT}$ would change by 20 mV.

E. Power Supply Rejection

For many published works on fully-integrated LDOs with fast transient responses, performance on power supply rejection is usually not discussed. However, PSR is the most important specification of an LDO designed for noise-sensitive loads. Supply ripples are mainly due to the output voltage ripples from the pre-stage DC-DC converter and on-chip noise generated by the digital/driver circuits. Ripples generated by DC-DC converters could be higher than 100 MHz, while noise generated by digital circuits is in the GHz range. To achieve good PSR, stacked power transistors were
used with large dropout voltages, sacrificing the LDO efficiency.

A TRI-Loop Full-Spectrum Power Supply Rejection Low-Dropout Regulator

Fig.13. Simulated load regulation with (W/L)\(_2\): (W/L)\(_3\) being set to 1:3 and 2:2, respectively; plus the case without Loop-3.

In this work, DC gain of Loop-1 has been sacrificed for fast transient response. Increase DC gain of Loop-1 needs additional stages that will introduce undesired LF poles. By setting \(P_{\text{out}}\) as the dominant pole, most of the silicon area (capacitance) can be effectively used to stabilize \(V_{\text{OUT}}\) and reject noise from \(V_{\text{IN}}\). The simulated PSR curves of the proposed LDO with and without a 100Ω \(R_L\) are shown in Fig. 14(a); and the PSR of the tri-loop regulator with and without \(C_B\), and the PSR of the regulator with only Loop-1 and \(C_B\), are plotted in Fig. 14(b), respectively. And, the equivalent model for the PSR of Loop-1 only is plotted in Fig. 14(c).

\[
\text{PSR}_{\text{Loop-1}} = \frac{V_{\text{out}}}{V_{\text{dd}}} = \frac{z_{\text{0-Loop-1}}}{r_{\text{dsP}} + r_{\text{dsP}} z_{\text{0-Loop-1}}} = \frac{1}{1 + \left(\frac{r_{\text{dsP}}}{C_L} + \frac{1}{r_{\text{dsP}} C_L}\right)} (23)
\]

The ultra-fast Loop-1 provides a shunt path \(z_{0\text{-Loop1}}\) for the output node. At medium and high frequencies, the light-load PSR is better than the full-load PSR, as \(C_L\) can more effectively bypass the ripple to ground when it is in parallel with a larger \(R_L\). Although, the ultra-fast Loop-1 could response to the input ripple in the VHF (very high frequency, 30 MHz–300 MHz) range with the assistance of \(C_L\), the LDO with Loop-1 only have poor PSR at low frequencies. Based on the Loop-1 PSR, 9 dB improvement on PSR is achieved at frequencies lower than 1MHz by the proposed tri-loop LDO. And, in FVF-based structures, \(V_{\text{OUT}}\) is mainly determined by \(V_{\text{SET}}\). Therefore, adding a bypass capacitor \(C_B\) (about 7 pF in this design) at the node could improve the PSR by filtering out the ripple that comes from \(V_{\text{MIR}}\) to \(V_{\text{OUT}}\). Adding \(C_B\) is effective in the medium frequency range (around 100 MHz to 1 GHz). Nevertheless, adding the \(C_B\) will lower the bandwidth of Loop-2 and -3, which is also the PSR corner frequency around 1 MHz. The long channel transistor \(M_{10}\) introduces an additional path from \(V_{\text{EN}}\) to \(V_G\) that slightly helping the PSR at high frequencies.

IV. RESULTS

Fig.15. The Line regulation waveform.

Fig.16. The Load regulation waveform.
Fig17. Waveform of the measured PSR up to 20GHz with load resistance 100ohms.

V. CONCLUSION

In this paper, a fully-integrated low-dropout regulator with fast transient response and full-spectrum PSR characteristics for wideband communication system is presented. Tri-loop architecture based on the flipped voltage follower and buffer impedance attenuation techniques is proposed and verified in 90nm CMOS process. With additional Loop-3, Vout DC accuracy is improved by 3 times compared to the conventional FVF-based LDO. Its distinct feature, ultra fast response time of 1.15ns and very low power consumption. This is the first attempt to design a fully-integrated LDO with certain PSR for the full-spectrum, while higher PSR is in demand for the future designs. As the FOM of this design scales with process, the proposed architecture will perform even better by using more advanced processes.

VI. REFERENCES