

Protection of Five Level H-Bridge MMC Based HVDC System Under DC- Side Faults

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Abstract: Two-level Voltage Source Converters (VSC) and Half-Bridge Modular Multilevel Converters (HBMMC) are most popular types of HVDC converters. One of their severe disadvantages is their unprotected nature to dc-side faults. The series connection of Double-Thyristor Switch Scheme (DTSS) across ac output terminals of the converter is the protection scheme for HVDC converters against dc-side faults. This scheme provides advantages such as lower dv/dt stresses, lower voltage rating of thyristor switches and complete segregation between the ac grid and converter during dc- side faults. In this paper, five-level Half-Bridge MMC with the series connection of DTSS has been proposed which gives better dv/dt stresses, voltage rating of thyristor switches, suppression of dc fault current and also faster response. Here, the simulation model for five-level HBMMC with series connection of DTSS has been designed and compare the results with two-level VSC and three-level HBMMC by using MATLAB/SIMULINK software.

Keywords: DC-Side Faults, Double Thyristor Switch, Protection of HVDC Converters, Voltage Source Converter (VSC), Modular Multilevel Converter (MMC).

I. INTRODUCTION

High Voltage Direct Current (HVDC) transmission system is an efficient technology to transmit bulk power over a long distances with low losses. The first commercial HVDC was installation in 1954. It is well suited for asynchronous interconnections and undersea cables. The fundamental process that occurs in an HVDC system is the conversion of electrical current from AC to DC (rectifier) and from DC to AC (inverter)[1]. The Voltage -Source Converter (VSC) is refer to as the building block of HVDC Technology which is applicable for interconnection of two very weak ac systems, offshore wind energy integration and DC grid expansion due to several advantages mainly no risk of commutation failure, flicker mitigation, less filters usage and faster dynamic response [2]-[4]. VSC operates with pulse width modulation (PWM) control at higher frequency when compared to the thyristor-based system. Because of higher frequency, the drawbacks of VSC system are electromagnetic compatibility/electromagnetic interference (EMC/EMI), transformer insulation stresses, and high frequency oscillations, which require additional filters [5]. The

conventional-Voltage Source Converter (2L-VSC) and Modular Multilevel Converter (MMC) based HVDC systems are popularly used for efficient grid integration. Both types provide: fast and independent control of active and reactive power (P&Q) flow in both directions and low harmonic generation hence the requirement of large filters is minimized[6],[7].

Compared to conventional 2-level VSC system, the topology of MMC offers some advantages:1) Low switching losses, low total harmonic distortion, modularity and scalability. 2) The currents in MMC arm and DC link are continuous, and the DC link capacitor can be omitted. 3) In a DC link short circuit fault, only some of sub-module (SM) capacitors are discharged and the discharging current is limited by the protection choke in the arms. Therefore, the system recovers fast.4) the system can remain operating for a certain period even when a few SM are out of order [8] - [11]. There are different MMC topologies like Half-Bridge MMC(HB-MMC), Full-Bridge MMC(FB-MMC), Cascade Two Level with Half-Bridge modules(HB-CTL) and Hybrid-MMC. Among those, Half-Bridge MMC is used because the reduced number of switches and cost, along with advances in power electronic technology. For DC short-circuit analysis, cells are modelled with specified IGBT switches, which characteristics include their short circuit withstand range [12]. In DC system, mainly faults are caused by one is malfunctioning of the equipment, controllers and another one is insulation failure due to external sources such as lightning, pollution, heavy wind, heavy rain and accumulation of snow and ice on transmission line etc. So protection of HVDC converter by limiting the fault currents is very important. Unfortunately, the classical VSCs and MMCs are defenseless against dc-side faults since their freewheeling diodes function as an uncontrolled rectifier bridge and feed the dc fault [13].

During the dc fault, the ac-side current contribution into the dc fault passes through the freewheeling diodes. As a result, the diodes may be damaged due to high fault current. This rectification mode of operation is shown in Fig. 1(a) and (b) for the two-level VSC and MMC during a dc-side fault. In Fig.1 (a), i_{f1} is the dc fault current which is summation of ac grid current (i_{gc}) and discharging current of the dc-link capacitor (i_{dis}). The discharging current has a

large first peak that decays with time [14]. In Fig. 1(b), the common dc-link capacitor is not utilized, which helps suppress the discharge current [15]. Here, ac grid current (i_{gc}) still exist that means there is no segregation between dc and ac sides during dc faults. Because of high cost and high conduction losses, dc circuit breaker (CB) may not be used to overcome the dc-side problems in HVDC converters. To achieve the required dc protection, AC CBs (ACCBs) may be used [16]. But freewheeling diodes should withstand the fault current until the CB trips the semiconductor devices may be damaged due to high fault currents. To improve the reliability of ac CBs in dc protection, converter embedded devices may be used in conjunction with the ac CBs [16].

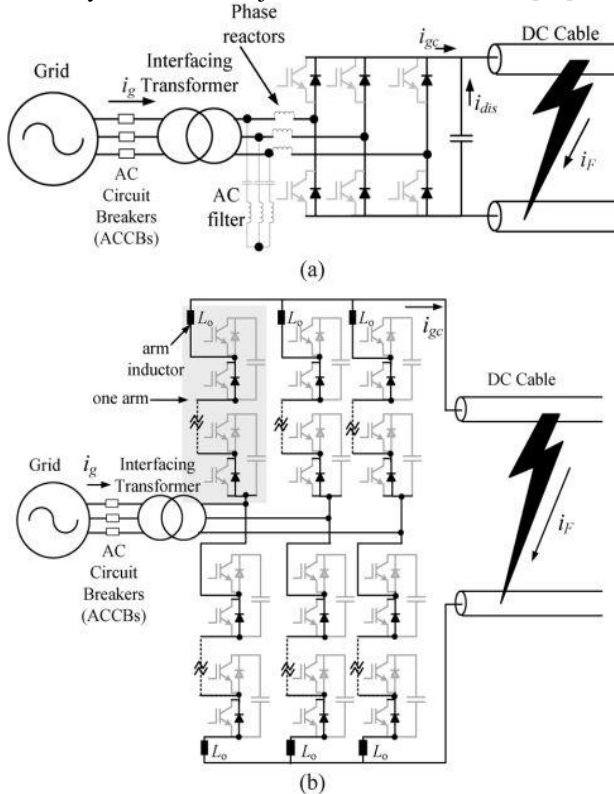


Fig. 1. HVDC converters during dc-side faults: (a) 2-level VSC and (b) MMC.

In the Single-Thyristor Switch Scheme (STSS) [16]–[18], a single thyristor switch is connected across each semiconductor device of the VSC and also each submodule of the MMC. By using this scheme, overcurrent stresses on semiconductor devices can be reduced due to sharing of fault current with thyristor and freewheeling diode. Compared to the freewheeling diode, the thyristor has high surge current withstand capability [18]. So, most of the fault current flows through the thyristor and not through the diode. The STSS protects the semiconductor devices but cannot prevent the grid current contribution into the dc fault. To overcome that problem, Double-Thyristor Switch Scheme (DTSS) is used [19]. In this scheme, a double-thyristor switch (back-to-back thyristor) is connected across each semiconductor device of the VSC and also each submodule of the MMC. The advantages of this scheme are protection of semiconductor

devices by sharing the fault current with the freewheeling diodes and simultaneously prevent the grid current contribution which allows the dc-link current to freely decay. The main disadvantages of this method are as follows:

- During normal operation, both thyristors have to withstand high dv/dt stresses which may produce capacitive displacement current in the device, which can cause undesirable turn on [20], [21].
- Due to overvoltage spikes and dv/dt , the semiconductor devices are damaged. So, a snubber circuit is also essential to prevent damage [20].
- The freewheeling diodes are still sharing the fault current with the thyristors.
- Complexity to design each MMC submodule with DTSS.

To overcome above problems another protection scheme is used, that is, series connection of DTSS switches across ac output terminals of the converter [23].

II. SERIES CONNECTION OF DTSS

The arrangement of series connection of Double-Thyristor Switch Scheme (DTSS) switches across ac output terminals of the converter is shown in Fig.2. Under normal operating condition, the thyristors are turned off. When a dc-side fault is initiated, the thyristors are turned on to segregate the HVDC converter from the ac side. By using this protection scheme, semiconductor devices of the converter are protected as well as eliminate the grid current contribution (i.e., complete segregation between the ac grid and dc side). In case of two-level VSC shown in Fig.3, the equivalent impedance (Z_{eq}) is same before and after firing the thyristors that means which is equal to interfacing impedance (Z_i). Thus, by turn on the thyristors, the required segregation will be achieved without increasing the magnitude of ac fault currents.

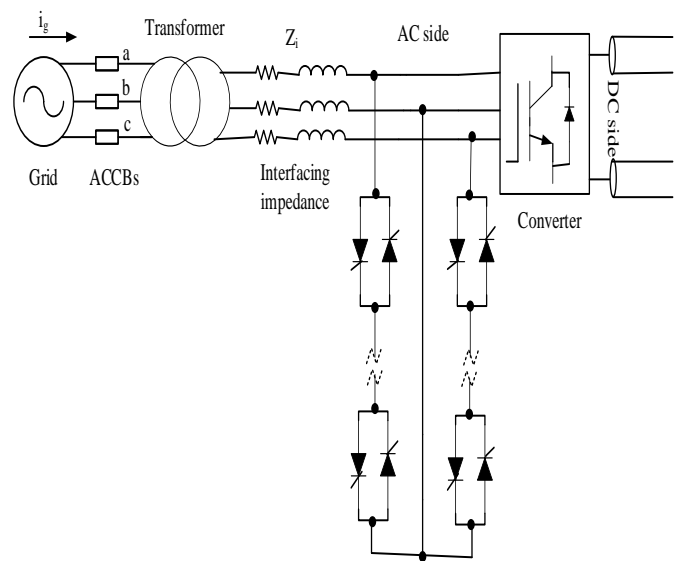


Fig.2. Series connection of DTSS against the dc-side faults.

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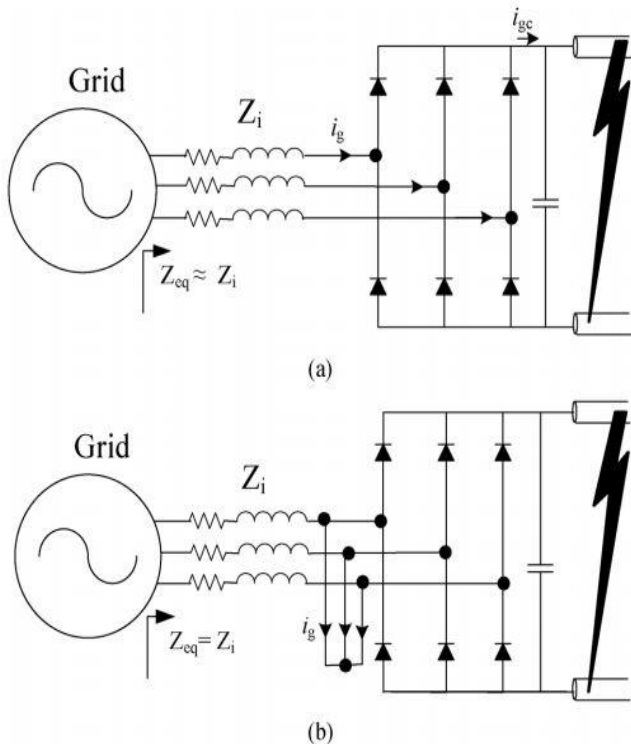


Fig.3. Effect of thyristors firing on the equivalent impedance seen by the grid, in 2-level VSC configuration: (a) before and (b) after thyristors firing.

In case of MMC shown in Fig.4, the equivalent impedance (Z_{eq}) during a dc-side fault after firing the thyristors [Fig. 4(b)] is lower than its value before firing [Fig. 4(a)] because of the arm inductors (L_o). The main two functions of the arm inductor (L_o) are limiting the fault currents and suppression of circulating currents [22]. The value of inductor will be low because the magnitude of ac current is not change during faulted condition. By using this scheme, the following advantages are gained [23].

- During dc faults, the complete segregation of ac grid and converter can be achieved.
- The magnitude of ac current is same before and after firing of the thyristor switches.
- The dc-link current is freely decay to zero. At that instant, disconnect the dc side fault carefully.
- This protection scheme can give thyristors with lower dv/dt stresses and lower voltage ratings.
- DC circuit breaker (DC CB) is not used because dc-link current is freely decay to zero.

A. dv/dt Stresses and Voltage Rating of the Required Thyristors

Thyristors are frequently exposed to a high rate of voltage change during operation. This produces a capacitive displacement current in the device, which can cause undesirable turn on. This is known as the dv/dt effect [20]. So, each device maintains its blocking capability (i.e., dv/dt capability). In Fig.2, The back-back thyristors are

combined and divided into two groups. For 2-level VSC and MMC, 3 and $3n$ back- back thyristor switches per group are required (where n is the number of sub- modules per arm). The converter line voltage is applied across each group.

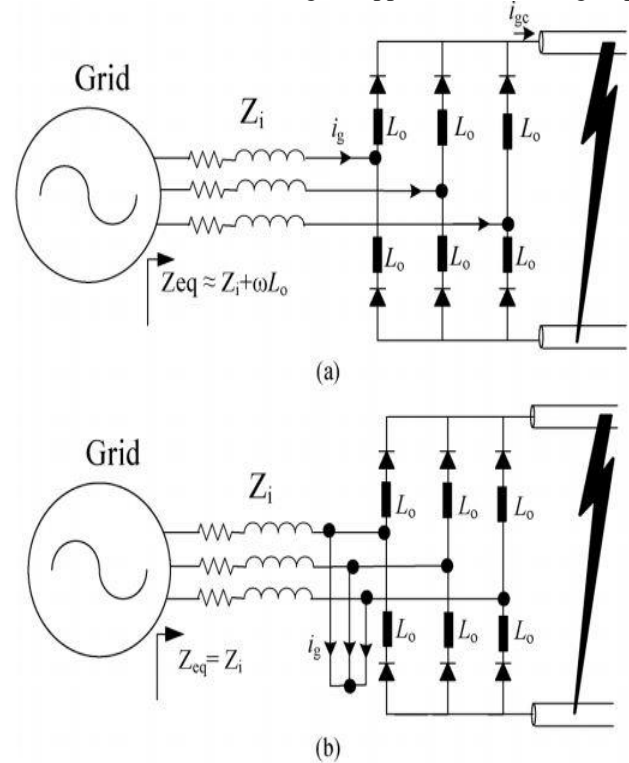


Fig.4. Effect of thyristors firing on the equivalent impedance seen by the grid in MMC configuration: (a) before and (b) after thyristors firing.

Conventional Two-Level VSC Case: During normal operating conditions, the voltage across semiconductor devices changes between 0 and V_{sw} . In this case, V_{sw} is equal to the dc-link voltage (V_{dc}). Now, $\pm V_{dc}$ is the voltage step with each change in converter line voltage is shared between three series back-to-back thyristor switches. The dv/dt stresses across each thyristor in case of 2-level VSC as follows:

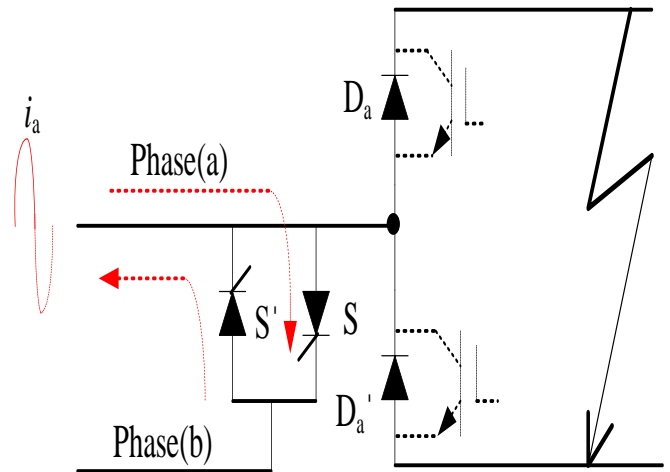


Fig. 5. AC current paths during the dc-side fault.

$$\frac{dv}{dt} \Big|_{2L-VSC} = \pm \frac{\left(\frac{V_{dc}}{3}\right)}{T_{on/off}} \quad (1)$$

Where $T_{on/off}$ is the time required for the semiconductor device to change its state from ON to OFF or vice-versa and V_{dc} is the highest instantaneous value of converter line voltage. This line voltage is shared by three series back-to-back thyristor switches, that means, the voltage rating of the each thyristor is $(V_{dc}/3)$ may be used.

MMC Case: In this case, V_{sw} is equal to the dc-link voltage (V_{dc}/n) . Now, $\pm V_{sw}$ is the voltage step with each change in converter line voltage is shared between $3n$ series back-to-back thyristor switches. The dv/dt stresses across each thyristor in case of MMC as follows:

$$\frac{dv}{dt} \Big|_{MMC} = \pm \frac{\left(\frac{V_{sw}}{3n}\right)}{T_{on/off}} = \pm \frac{\left(\frac{V_{dc}}{3n^2}\right)}{T_{on/off}} \quad (2)$$

The highest instantaneous value of converter line voltage (V_{dc}) is shared by $3n$ series back-to-back thyristor switches, that is, the voltage rating of the each thyristor is $(V_{dc}/3n)$ may be used.

Three-level MMC: For three-level MMC (3L-MMC), number of sub-modules per arm (n) is equal to 2. The dv/dt stresses across each thyristor in case of 3L-MMC as follows:

$$\frac{dv}{dt} \Big|_{3L-MMC} = \pm \frac{\left(\frac{V_{dc}}{3n^2}\right)}{T_{on/off}} \quad (3)$$

The voltage rating of the each thyristor is $(V_{dc}/3n)$, that is equal to $(V_{dc}/6)$ may be used.

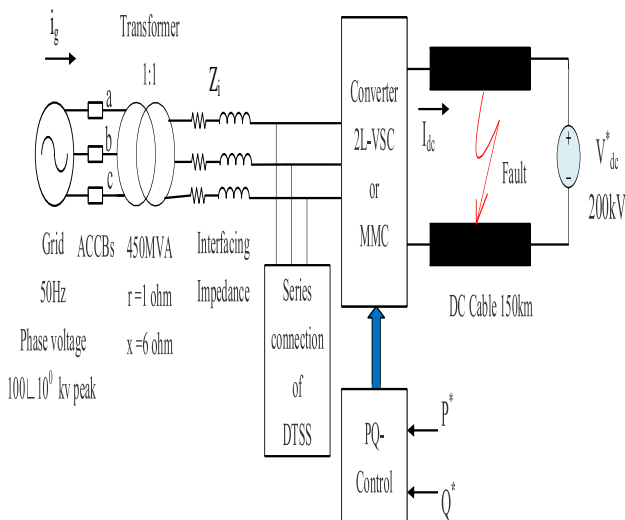


Fig.6. Block diagram for the simulated HVDC system.

B. Current Rating of the Required Thyristors

During dc-side fault, the per-phase path of ac current as shown in Fig.5. In case of series connection of DTSS across ac output terminals of the HVDC converter, the total amount of ac current flows through the thyristors as shown in Fig.6. The steady-state currents of thyristors and diodes during a dc fault are given by (4) and (5), respectively.

$$i_{T_1} = i_a^+, i_{T_2} = i_a^- \quad (4)$$

$$i_{D_1} = 0, i_{D_2} = 0 \quad (5)$$

Where i_a^+ and i_a^- are the positive and the negative currents of phase “a”. From above equations it is clear that the current rating of the thyristors will be high compared to STSS and DTSS because they carry the full ac current. For 2L-VSC and 3L-MMC configurations, the current rating of each thyristor is I_{sc} . Where I_{sc} is the magnitude of ac current during dc-side faults.

TABLE I: Parameters of HVDC System Model

AC Side	
Rated (Base) Power	450 MVA
Grid phase voltage	100 KV(peak)
Rated (Base) AC phase current	3000 A(peak)
Three-phase transformer ratio	1:1
Active power reference	430 MW
Reactive power reference	-100 MVAR
Transformer resistance	1 Ω
Transformer reactance	6 Ω
DC Side	
Rated (Base) DC voltage, V_{dc}	200 KV
Rated (Base) DC current	2250 A
DC cable length	150 km
DC cable resistance	14 mΩ / km
DC cable inductance	0.1 mH / km
2-level VSC	
DC-link capacitor	100 μF
3-level MMC	
Arm inductor, L_0	3 mH
Sub-module(SM) capacitance	100 μF
5-level MMC	
Arm inductor, L_0	5 mH
Sub-module(SM) capacitance	200 μF

III. PROPOSED SCHEME

Five level Half-Bridge Modular Multilevel Converter (5L-HBMMC) with series connection of DTSS across ac output terminals of the HVDC converter has been proposed due to following benefits are gained.

- Lower dv/dt stresses and lower voltage rating of the thyristor switches.

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- The performance of dc fault current suppression capability can be improved.
- Low switching losses because of the lower switching frequency compared to 2L-VSC and 3L-MMC respectively.
- Fast response in addition to get complete segregation between ac grid and converter during dc-side fault.

The general diagram of MMC is shown in Fig.1(b) and also the Simulink model for 5L-HBMMC is shown in Fig.7. In case of five-level HBMMC, the number of sub-modules per arm (n) is equal to 4 and the number of series connected back-to-back. Thyristor switches in each group (3n) is equal to 12. The dv/dt stresses across each thyristor in case of 5L-HBMMC as follows:

$$\left. \frac{dv}{dt} \right|_{5L-MMC} = \pm \frac{\left(\frac{V_{dc}}{3n^2} \right)}{T_{on/off}} \quad (6)$$

Where $n = 4$. The highest instantaneous value of converter line voltage (V_{dc}) is shared by $3n$ series back-to-back thyristor switches, that is, the voltage rating of the each thyristor is $(V_{dc}/3n)$, that is equal to $(V_{dc}/12)$ may be used. The current rating of thyristor is I_{sc} . Here I_{sc} is the magnitude of ac current during dc-side fault which is not changed (in case of 2L-VSC, 3L-MMC and 5L-MMC) because of series connection of back-to-back thyristor switches across ac output terminals of the converter.

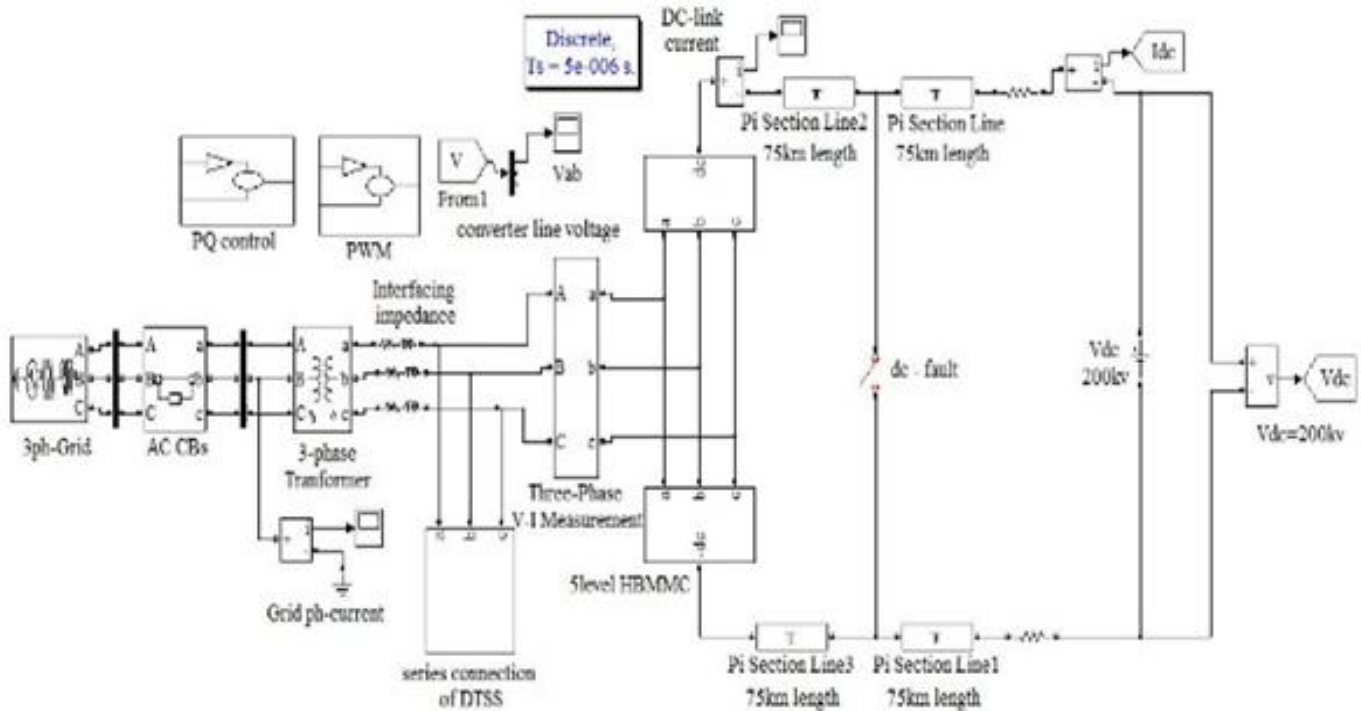


Fig.7. Simulink diagram for 5L-HBMMC.

TABLE II: Comparison between the Proposed Scheme and Existing Schemes

Type of Scheme	Converter Type	dv/dt stresses across each thyristor (kV/ μ s)	Voltage rating of the thyristor (kV)
Existing Schemes	2-level VSC	66.66	66.66
	3-level MMC	16.66	33.33
Proposed Scheme	5-level MMC	4.17	16.66

IV. DC FAULT CURRENT AND COMPARISON OF DV/DT STRESSES

A. DC Fault Current

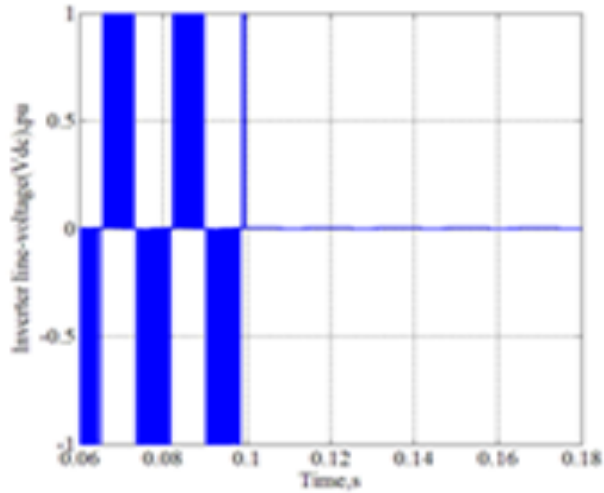
This section shows the dc-side performance of the 2L-VSC and MMC-based HVDC systems. The protection scheme (series connection of DTSS) provide complete segregation between the ac and dc sides during dc-side faults.

1. Two-Level VSC: The Dc Fault Current Will Behave As In Stage I and II.

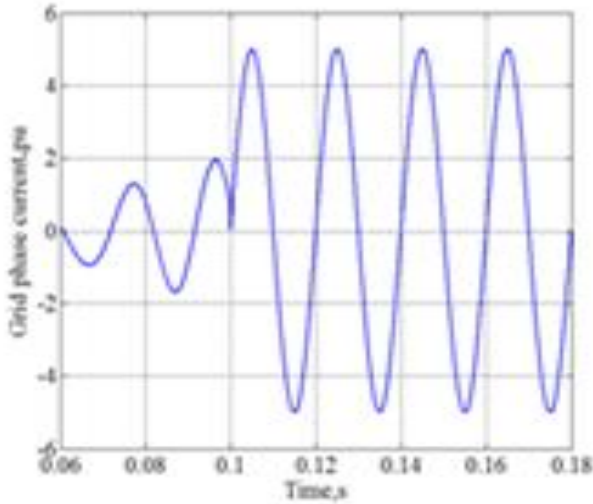
Stage I: Capacitor discharge stage: Throughout this stage, the dc-link capacitor starts discharging. The discharge current has a high peak and decays with time.

Stage II: Diode freewheel stage: This stage is started as the dc fault commutates to the converter freewheeling diodes when the dc-link voltage reaches zero and the cable inductance drives the current around the freewheeling path.

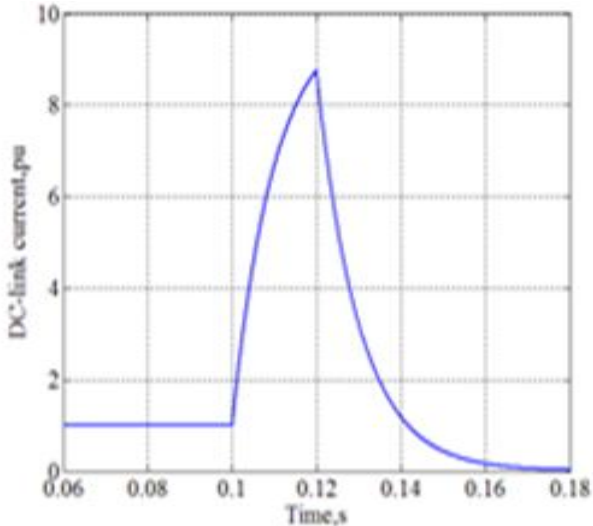
At this stage, the initial diode currents are high which may damage them, then the current decays with time. This permits the dc-link current to decay freely to zero (dc fault current suppression capability).



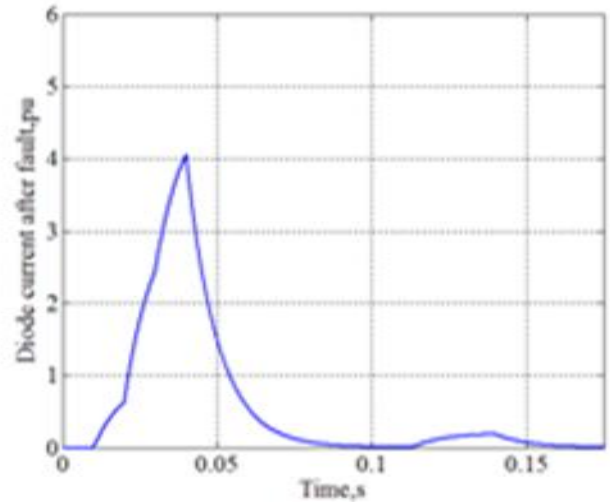
(a)



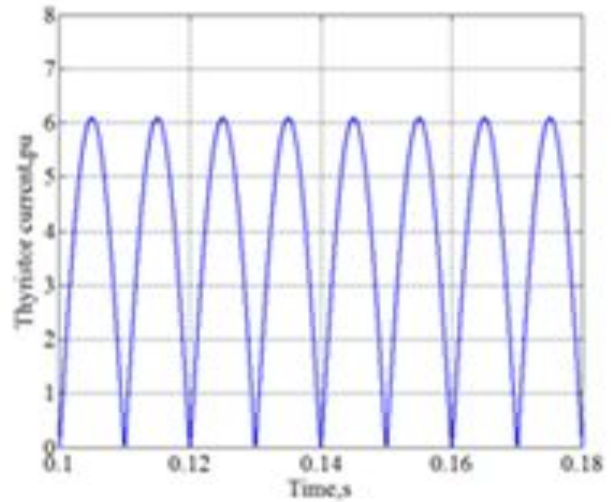
(b)



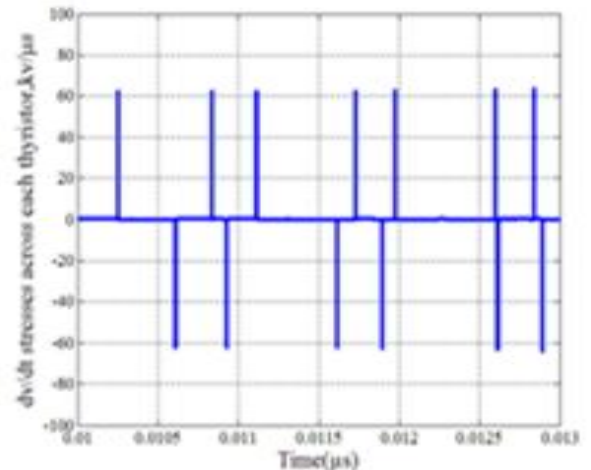
(c)



(d)



(e)



(f)

Fig.8. Simulation results for the two-level VSC with series connection of DISS (a) converter line voltage, (b) per-phase grid current, (c) dc-link current, (d) freewheeling diode current (e) thyristors currents during the dc fault, and (f)dv/dt stresses across each thyristor during normal operating conditions.

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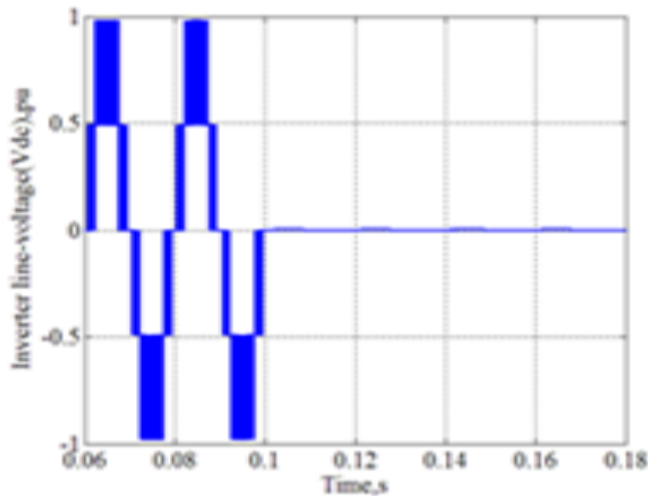
2.Three-level MMC and 5L-MMC: The dc-link capacitors are no longer connected to the dc side during dc faults [Fig. 1(b)] that means, under dc fault conditions there is no discharge currents are flowing. Upon fault beginning, the diode freewheeling stage (Stage II) is initiated as the cable inductance energies the current around the freewheeling path dissipating its energy in the cable resistance. The current will have an exponential current decay until reaching zero (dc fault current suppression capability).

B. Comparison between the Proposed Scheme and Existing Schemes

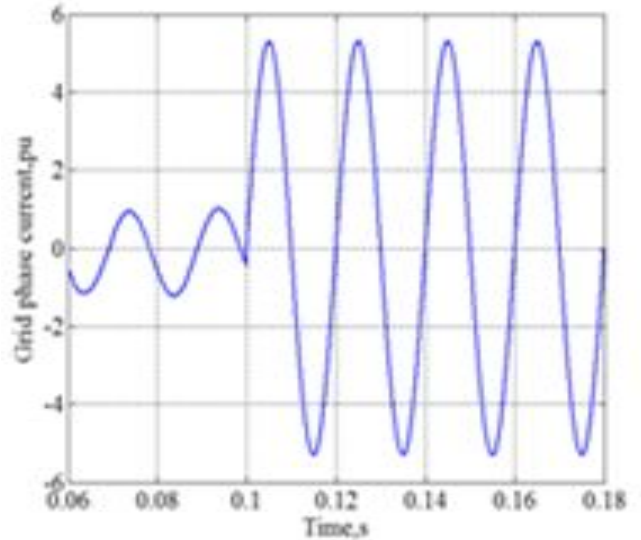
The Table II shows that the comparison between existing schemes and the proposed scheme in terms of dv/dt stresses and voltage ratings of the required thyristors based on the equations (1),(2),(3) and(6). From Table II, the proposed scheme (i.e., five level Half-Bridge MMC with series connection of DTSS) gives lower dv/dt stresses and lower voltage ratings of the required thyristors comparing to 2L-VSC and 3L-MMC respectively. By using the proposed scheme, the following points can be concluded:

- The dv/dt stresses are reduced from $66.66 \text{ kV}/\mu\text{s}$ to $4.17 \text{ kV}/\mu\text{s}$ and also voltage ratings of the necessary thyristors are reduced from 66.66 kV to 16.66 kV comparing to two-level VSC.
- The dv/dt stresses are reduced from $16.66 \text{ kV}/\mu\text{s}$ to $4.17 \text{ kV}/\mu\text{s}$ and also voltage ratings of the necessary thyristors are reduced from 33.33 kV to 16.66 kV comparing to three-level MMC. That means by using 5L-HBMMC,
- The % dv/dt stresses are reduced by 93.74% and also percentage of voltage ratings of the necessary thyristors are reduced by 75% comparing to the 2L-VSC.
- The % dv/dt stresses are reduced by 74.96% and also percentage of voltage ratings of the required thyristors are reduced by 50% comparing to the 3L-MMC.

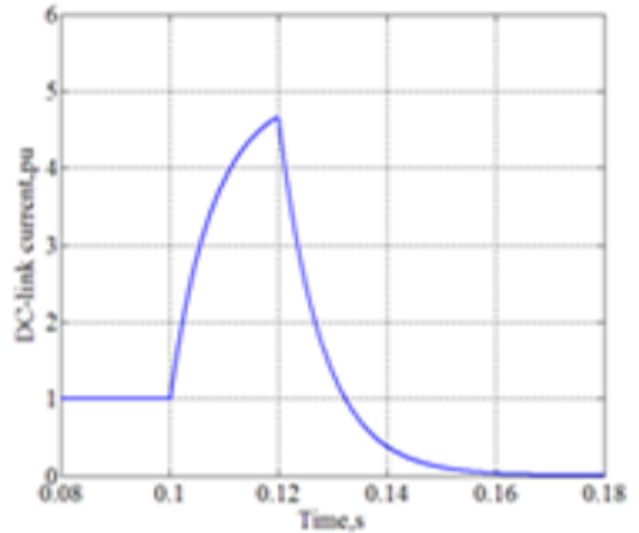
In case of existing schemes and proposed scheme, the current rating of necessary thyristors (I_{sc}) is same because of series connection of DTSS across ac output terminal of the converter.



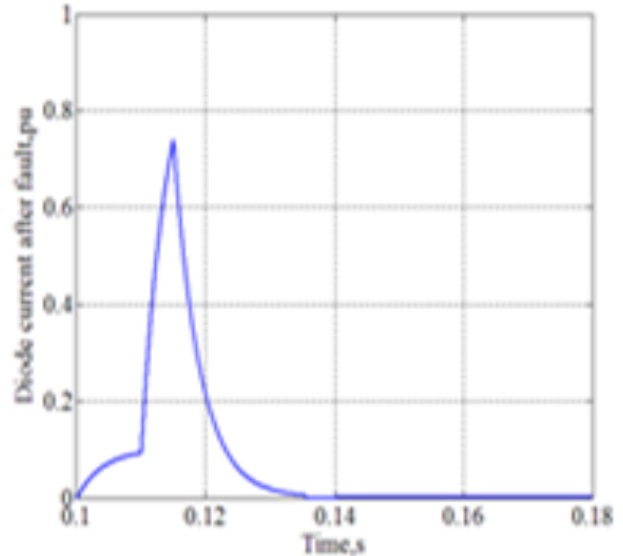
(a)



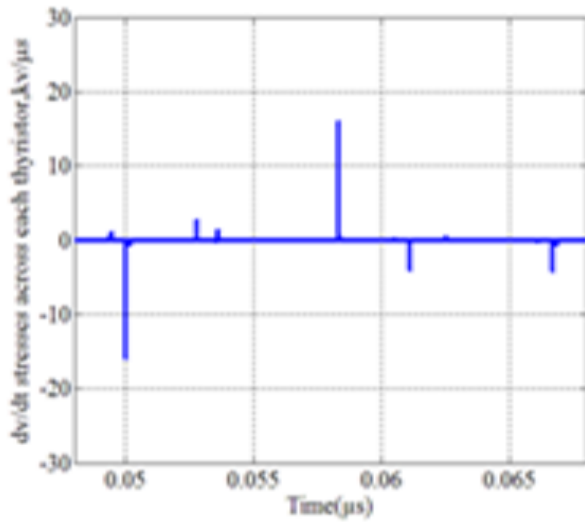
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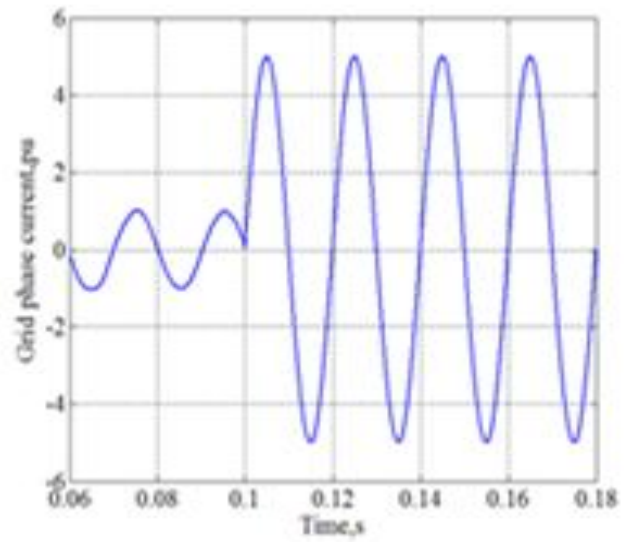
(c)



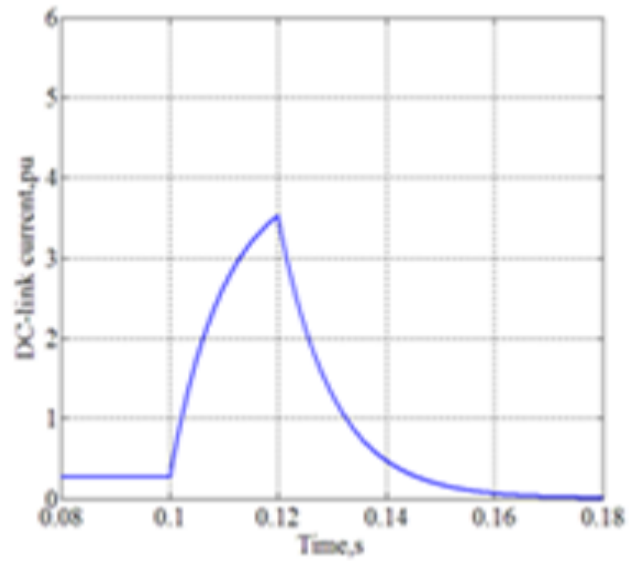
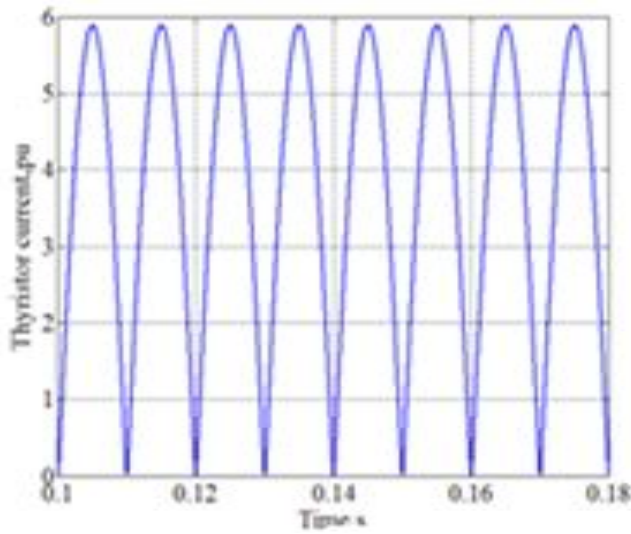
(d)



(e)

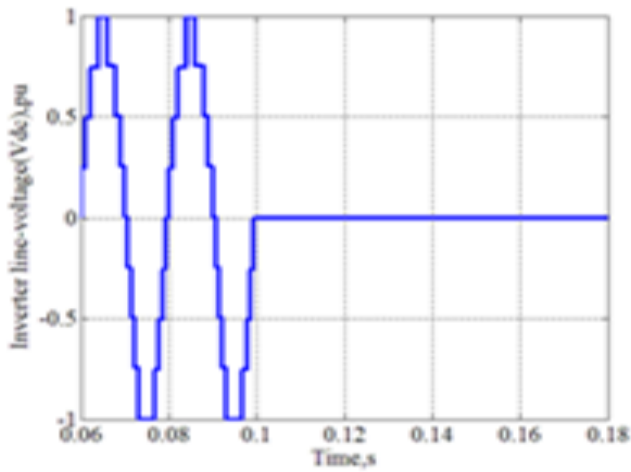


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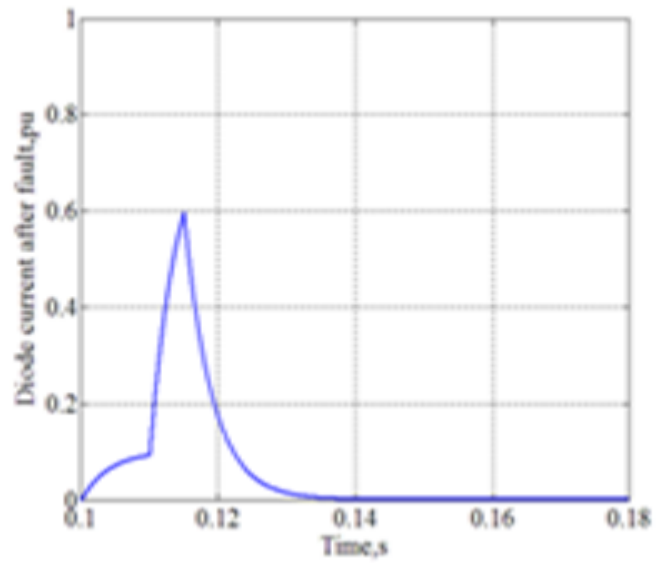


(C)

Fig.9. Simulation results for the three-level MMC with series connection of DISS (a) converter line voltage, (b) per-phase grid current, (c) dc-link current, (d) freewheeling diode current (e) thyristor currents during the dc fault, and (f)dv/dt stresses across each thyristor during normal operating conditions.

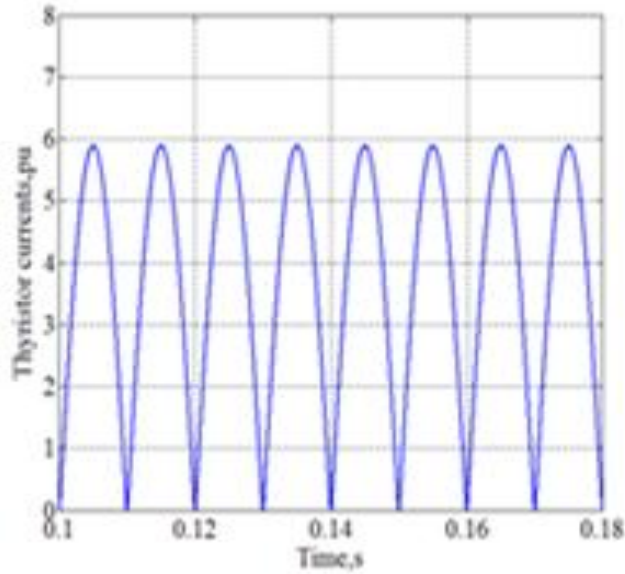


(a)

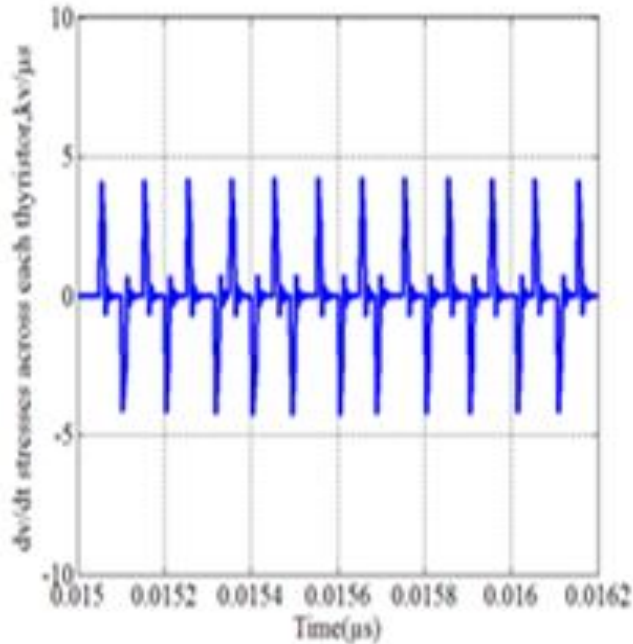


(d)

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(e)



(d)

Fig.10. Simulation results for the five-level MMC with series connection of DISS (a) converter line voltage, (b) per-phase grid current, (c) dc-link current, (d) freewheeling diode current (e) thyristors currents during the dc fault, and (f) dv/dt stresses across each thyristor during normal operating conditions.

V. SIMULATION RESULTS

The block diagram for the simulated HVDC system is shown in Fig. 6. The parameters of the HVDC system are given in Table I. Three simulation models such as existing schemes (2L-VSC and 3L-MMC) and proposed scheme (5L-MMC) with series connection of DTSS across ac output terminals of the HVDC converter have been developed. During normal operating conditions, power-quality (PQ)

control is applied, and at 0.1s, a dc fault is initiated at the midpoint of the dc cable. The simulation results for two-level VSC, 3L-MMC and 5L-MMC with series connection of DTSS are shown in Fig. 8, 9 and 10, respectively. Figs.8 (a), 9(a) and 10(a) show the converter line voltage during normal operation and a dc- side fault. The line voltage is forced to zero in order to provide full segregation between the ac and dc sides. Figs.8 (b), 9(b) and 10(b) show the effect of a dc-side fault on the ac current. It is clear that, the steady-state magnitude of ac current during a dc fault does not affect. The dc-link currents of the two-level VSC, three-level MMC and five-level MMC are shown in Figs.8(c), 9(c) and 10(c), respectively. This results provide no grid contribution stage and the dc current decays freely to zero. So, for clearing the fault, the cable can be disconnected carefully from the converter dc terminals by using simple dc switch. Figs.8 (d), 9(d) and 10(d) show the diode currents for the two level VSC, 3L-MMC and 5L-MMC, respectively. The steady-state diode currents are zero, that is, it offers complete segregation of the converter and its semiconductor switches. Figs.8 (e), 9(e) and 10(e) show the thyristor currents for the 2L-VSC, 3L-MMC and 5L-MMC, respectively. As expected, the thyristor currents are higher because they carry the full current and do not share it with diodes as in STSS or DTSS. Finally, Figs.8 (f), 9(f) and 10(f) show that with the help of the proposed scheme(5L-MMC), the % dv/dt stresses are reduced by 93.74% comparing to 2L-VSC and also the % dv/dt stresses are reduced by 74.96% comparing to 3L-MMC systems, respectively.

VI. CONCLUSION

In this paper, five levels Half-Bridge Modular Multilevel Converter (5L-HBMMC) with series connection of Double Thyristor Switch Scheme (DTSS) is proposed. From results it is conclude that, the proposed scheme gives better results such as lower dv/dt stresses, lower voltage rating of thyristor switches and better dc fault current suppression capability comparing with two-level VSC and three-level MMC systems respectively and also to providing full segregation between the converter semiconductor devices and ac grid during dc-side faults. By using proposed scheme (5L-MMC), the% dv/dt stresses are reduced by 74.96% and also the voltage ratings of required thyristors are reduced by 50% comparing with three-level MMC systems.

VII. REFERENCES

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