International Journal of Advanced Technology and Innovative Research

ISSN 2348–2370
Vol.07,Issue.11,
August-2015,
Pages:2041-2047

www.ijatir.org

Simulation of Three-Phase Multilevel Inverter with Reduced Switches for Induction Motor Applications

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Abstract: The proposed topology significantly reduces the number of dc voltage sources, switches, IGBTs, and power diodes as the number of output voltage levels increases. To synthesize maximum levels at the output voltage, the proposed topology is optimized for various objectives, such as the minimization of the number of switches, gate driver circuits and capacitors, and blocking voltage on switches. This new type of converter is suitable for high voltage and high power applications. This multilevel inverter has ability to synthesize waveforms with better harmonics spectrum. The power loss in the circuit is less due to less number of switches. There are numerous topologies has been introduced and widely studied for utility and drive application. In this paper, a study of 15 -level inverter using less number of switches as compare to the technologies previously developed. When we increases the level of inverter then we gets the high output voltage and the stress of each switch is also reduces means each switches faces low value of dv/dt. The output waveform of multilevel inverter follows the sinusoidal waveform hence the harmonic contents are less. However as the number of output level increases, the circuit becomes bulky due to the increase in the number of power devices. It is proposed to employ a new technique to obtain a multilevel output using less number of power semiconductor switches. The objective of this paper is to make the easy cheap and good multilevel inverter with less number of switches and understanding the working and simulation of a 15-level with the proposed converter topology using less number of switches using MATLAB/SIMULINK software.

Keywords: Matlab Simulink, Multi Level Inverter.

I. INTRODUCTION

The voltage source inverters produce a voltage or a current with levels either 0 or ±V dc they are known as two level inverters. To obtain a quality output voltage or a current waveform with a minimum amount of ripple content, they require high switching frequency along with various pulse width modulation (PWM) strategies. In high power and high voltage applications, these two level inverters, however, have some limitations in operating at high frequency mainly due to switching devices should be used in such a manner as to avoid problems associated with their series- parallel combinations that are necessary to obtain capability of handling high voltages and currents. It may be easier to produce a high power, high voltage inverter with the multi-level structure because of the way in which device voltage stresses are controlled in the structure. Increasing the number of voltage levels in the inverters without requiring higher ratings on the individual devices can increase the power rating. The unique structure of Multi-level voltages sources inverters allow them to reach high voltages with low harmonics without the use of transformer or series connected synchronized switching devices. As the number of voltage levels increases, the harmonic content of output voltage waveform decreases significantly.

II. EXISTING BASIC TOPOLOGIES

The general structure of multi-level converter is to synthesize a near sinusoidal voltage from several levels of dc voltages, typically from capacitor voltage sources. As number of levels increases, the synthesized output waveform has more steps, which provides a staircase wave that approaches a desired waveform. Also, as steps are added to waveform, the harmonic distortion of the output wave decreases, approaching zero as the number of voltage levels increases. The Multi-level inverters can be classified into three types. [1]– [4].

- Diode-clamped or neutral point clamped topology(NPC)
- Capacitor clamped or flying capacitor clamped topology
- Cascaded H-bridge topology

A. Diode- clamped multi – level inverter

A diode – clamped (m-level) inverter (DCMLI) as shown in Fig.1 typically consists of (m-1) capacitor on the dc bus and produces m levels on the phase voltages. Figure shows full bridge five-level diode clamped converter. The numbering order of the switches is Sa1, Sa2, Sa3, Sa4, S'a1, S'a2, S'a3, S'a4. The dc bus voltage consists of four capacitors C1, C2, C3, and C4. For a dc voltage Vdc, the voltage across each capacitor is Vdc/4, and each devices voltage stress is limited to one capacitor voltage level V dc/4 through clamping diodes. An m-level inverter leg requires (m-1) capacitors, 2(m-1) switching devices and (m-1) X (m-1) clamping diodes. [5].

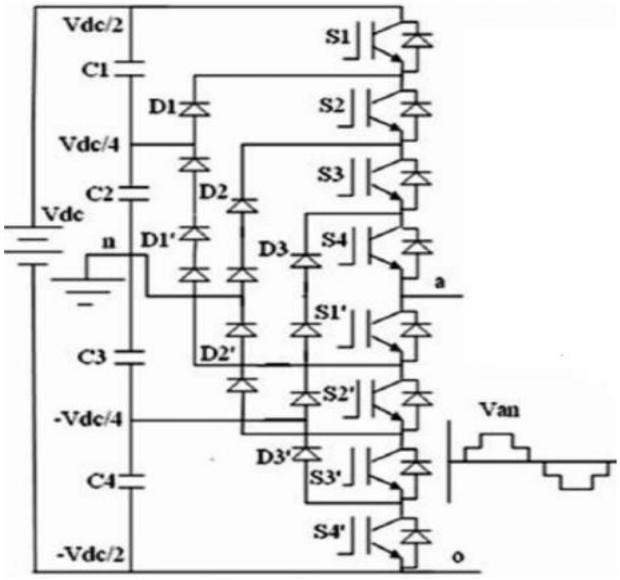

Fig.1. Single phase Diode clamped inverter.

The main drawbacks of NPC topology are their unequal voltage sharing among series connected capacitors that result in dc-link capacitor unbalancing and requiring a great number of clamping diodes for higher levels.

B. Flying Capacitor Multilevel Inverter

The fig2 shows a single phase full bridge 5-level inverter based on flying capacitors. Each phase like has an identical structure. Assuming that each capacitor has the same voltage rating, the series connection of the capacitors indicates the voltage level between calming points. All phase legs share the DC link capacitors C1 to C4. [6]

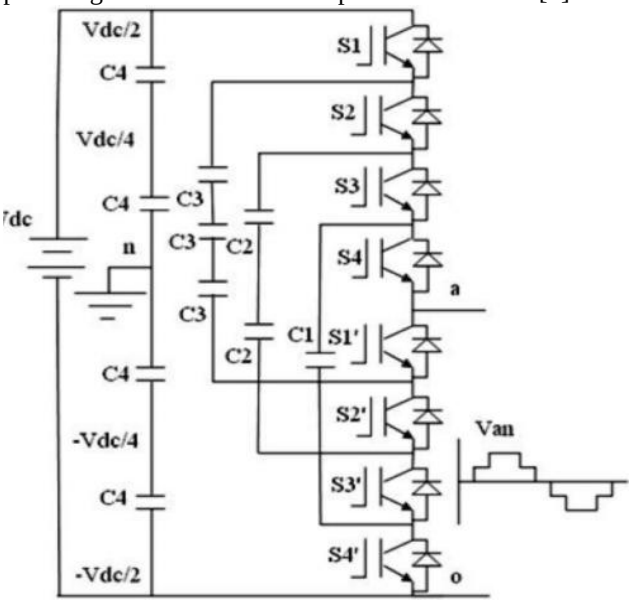

Fig.2. Single Phase Flying Capacitor Inverter

The FC multilevel converter uses flying capacitor as clamping devices. These topologies have several attractive properties in comparison with the NPC converter, including the advantage of the transformer less operation and redundant phase leg states that allow the switching stresses to be equally distributed between semiconductor switches [8], [9]. But, these converters require an excessive number of storage capacitors for higher voltage steps.

C. Cascaded Multi-Level Inverter

A relatively new converter structure called Cascaded Multi-level inverter, can avoid extra clamping diodes or voltage balancing capacitors. The converter topology used here is based on the series connection of single phase inverters with separate DC sources .The different topologies by which h-bridge are designed are Cascaded H-bridge: Figure 3 shows the basic block of cascade H-bridge Multi-level inverter and its associated switching instants. As shown it consists of four power devices and a DC source. The switching states for four power devices are constant i.e., When S1 is on, S2 cannot be on and vice versa. Similarly with S3 and S4.

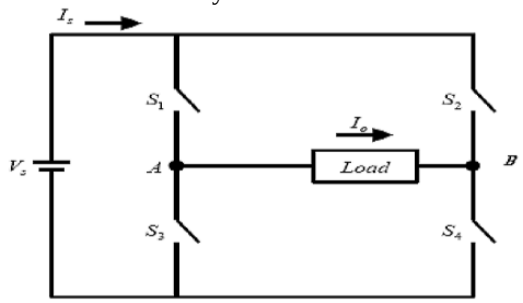

Fig.3. Block of a H-bridge Multi-level inverter.

Fig4 shows the power circuit for one phase of multi-level inverter. The resulting voltage ranges from +3Vdc to -3Vdc and the staircase are nearly sinusoidal, even without filtering.

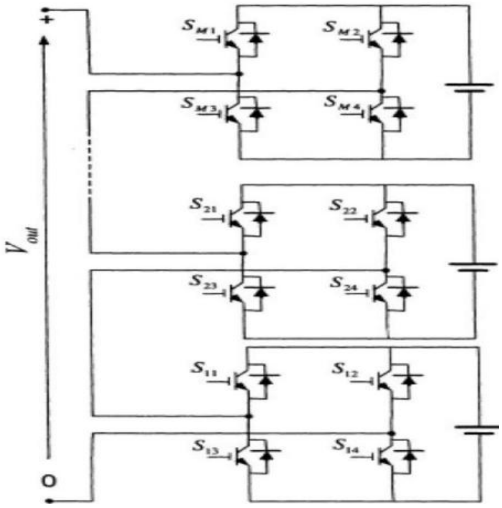

Fig .4.Circuit diagram of 4-level cascade multi-level inverter Hybrid.

H-bridge: A hybrid H-bridge inverter consists of a series of H-bridge inverter units. The general function of this Multi-level inverter is to synthesize a desired voltage form several DC sources (SDCSs). Each SDCS is connected to an H-bridge inverter. The AC terminal voltages of different level inverters are connected in series. Unlike diode clamp or flying capacitors inverters the hybrid H-bridge inverter does not require any voltage clamping diodes or voltage-balancing capacitors. Hybrid multilevel converters have been presented

in [12], [13]. In the hybrid topologies, the dc voltage sources magnitudes are unequal or changed dynamically [14]. These converters reduce the size and cost of the converter and improve the reliability since less number of semiconductors and capacitors are used in this topology [15]. The hybrid multilevel converters comprises of different multilevel topologies which are having unequal values of dc voltage sources and different modulation techniques [12]. With appropriate selection of switching devices, the converter cost is significantly reduced. But, the application of different multilevel topologies result in loss of modularity and produces problems with switching frequency and restrictions on the modulation and control method [16].

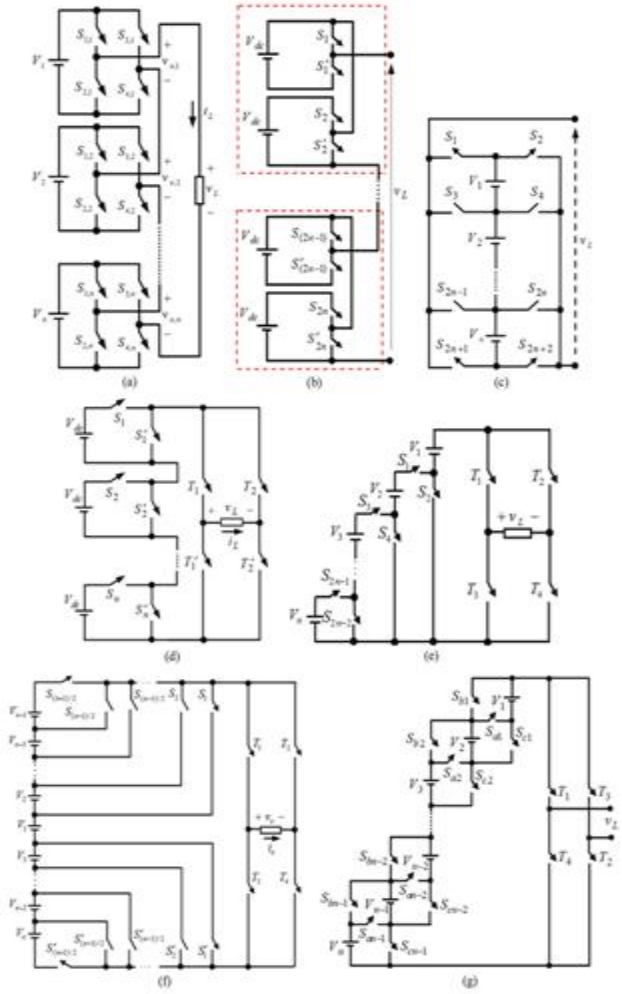

Fig.5. Cascaded multilevel inverters. (a) Conventional cascaded multilevel inverter R2 for V1 = V2 = • • • = Vn = Vdc [14], R3 for V1 = Vdc, V2 =• • • = Vn = 2Vdc [12], and R4 for V1 = Vdc, V2 = • • • = Vn = 3Vdc [20]. (b) Presented topology in [17], with R7 for V1 = V2 = • • • = Vn = Vdc. (c) Presented topology in [19], with R8 for V1 = V2 = • • • = Vn = Vdc and R9 for V1 = Vdc, V2 = • • • = Vn = 2Vdc. (d) Presented topology in [18] with R10. (e) Presented topology in [16], with R6 for V1 = V2 = • • • =Vn = Vdc. (f) Presented topology in [15], with R5 for V1 = V2 = • • • = Vn =Vdc. (g) Presented topology in [13], with R1 for V1 = V2 = • • • = Vn = Vdc.

D. Comparing the Proposed Topology with the Conventional Topologies

The main aim of introducing the developed cascaded inverter is to increase the number of output voltage levels by using the minimum number of power electronic devices. Therefore, several comparisons are done between the developed proposed topology and the conventional cascaded inverters from the numbers of IGBTs, driver circuits, and dc voltage sources points of view. In addition, the maximum amount of the blocked voltage by the power switches is also compared between the proposed inverter and the other presented topologies. In this comparison, the proposed cascaded inverter that is shown in 5(b) with its proposed algorithms is represented by P1 to P4, respectively. In [13], a symmetric cascaded multilevel inverter has been presented that is shown by R1 in this comparison. The H-bridge cascaded multilevel inverter has been presented in [14]. This inverter is represented by R2. In addition, two other algorithms have been presented for the H-bridge cascaded inverter in [12] and [20] that are represented by R3 and R4, respectively. In [15]–[17], three other symmetric cascaded multilevel inverters have been presented. These inverters are shown by R5−R7, respectively. The other cascaded multilevel inverter with two different algorithms has been presented in [19]. This inverter with its algorithms is represented by R8 and R9, respectively. Another symmetric cascaded multilevel inverter that has been presented in [18] is represented by R10 in this comparison. Fig. 5 indicates all of the aforementioned cascaded multilevel inverters.

III. PROPOSED TOPOLOGY

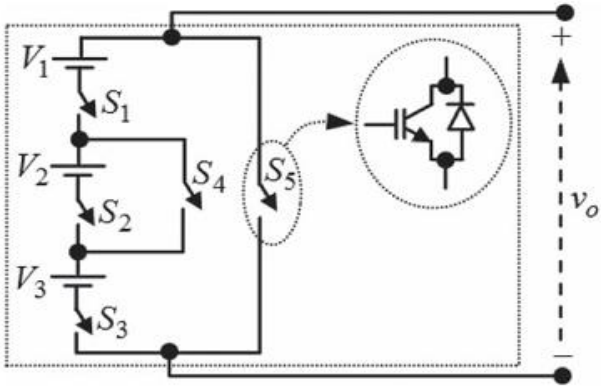

Fig.6.Proposed Basic Unit.

Table I. Permitted turn on and off states for Switches in the proposed basic unit

state	Switches state					v_o
	S_1	S_2	S_3	S_4	S_5	
1	off	off	off	off	on	0
2	on	off	on	on	off	V_1+V_3
3	on	on	on	off	off	$V_1+V_2+V_3$

Fig.6 shows the proposed basic unit. As shown in Fig. 6, the proposed basic unit is comprised of three dc voltage sources and five unidirectional power switches. In the proposed

structure, power switches (S_2, S_4), (S_1, S_3, S_4, S_5), and (S_1, S_2, S_3, S_5) should not be simultaneously turned on to prevent the short circuit of dc voltage sources. The turn on and off states of the power switches for the proposed basic unit are shown in Table I, where the proposed basic unit is able to generate three different levels of 0, $V_1 + V_3$, and ($V_1 + V_2 + V_3$) at the output. It is important to note that the basic unit is only able to generate positive levels at the output. It is possible to connect n number of basic units in series. As this inverter is able to generate all voltage levels except V_1, it is necessary to use an additional dc voltage source with the amplitude of V_1 and two unidirectional switches that are connected in series with the proposed units. The proposed cascaded inverter that is able to generate all levels is shown in Fig. 5(a). In this inverter, power switches S_1' and S_2' and dc voltage source V_1 have been used to produce the lowest output level. The amplitude of this dc voltage source is considered $V_1 = V_{dc}$ (equal to the minimum output level). The output voltage level of each unit is indicated by $v_{o,1}$, $v_{o,2}$. . . $v_{o,n}$, and vo. The output voltage level vo of the proposed cascaded multilevel inverter is equal to

$$v_o(t) = v_{o,1}(t) + v_{o,2}(t) + \cdots + v_{o,n}(t) + v_o'(t). \quad (1)$$

The generated output voltage levels of the proposed inverter are shown in Table II. As aforementioned and according to Table II, the proposed inverter that is shown in Fig. 5(a) is only able to generate positive levels at the output. Therefore, an H-bridge with four switches T1–T4 is added to the proposed topology. This inverter is called the developed cascaded multilevel inverter and is shown in.fig.7. If switches T1 and T4 are turned on, load voltage vL is equal to vo, and if power switches T2 and T3 are turned on, the load voltage will be −vo. For the proposed inverter, the number of switches Nswitch and the number of dc voltage sources Nsource are given by the following equations, respectively

$$N_{\text{switch}} = 5n + 6 \quad (1)$$

$$N_{\text{source}} = 3n + 1 \quad (2)$$

Table II. Generated Output Voltage Levels Vo Based on the Off and On States of Power Switches

v_o	S_1'	S_2'	$S_{1,1}$	$S_{2,1}$	$S_{3,1}$	$S_{4,1}$	$S_{5,1}$	$S_{1,2}$	$S_{2,2}$	$S_{3,2}$	$S_{4,2}$	$S_{5,2}$	⋯	$S_{1,n}$	$S_{2,n}$	$S_{3,n}$	$S_{4,n}$	$S_{5,n}$
0	off	on	off	off	off	off	on	off	off	off	off	on	⋯	off	off	off	off	on
V_1	on	off	off	off	off	off	on	off	off	off	off	on	⋯	off	off	off	off	on
$V_{1,1}+V_{3,1}$	off	on	on	off	on	on	off	off	off	off	off	on	⋯	off	off	off	off	on
$V_{1,1}+V_{2,1}+V_{3,1}$	off	on	on	on	on	off	off	off	off	off	off	on	⋯	off	off	off	off	on
$V_{1,2}+V_{3,2}$	off	on	off	off	off	off	on	on	off	on	on	off	⋯	off	off	off	off	on
$V_{1,2}+V_{2,2}+V_{3,2}$	off	on	off	off	off	off	on	on	on	on	off	off	⋯	off	off	off	off	on
$V_{1,1}+V_{1,2}+V_{1,3}+V_{2,1}+V_{2,3}$	off	on	on	on	on	off	off	on	off	on	on	off	⋯	off	off	off	off	on
$V_{1,1}+V_{1,2}+V_{1,3}+V_{2,1}+V_{2,2}+V_{2,3}$	off	on	on	on	on	off	off	on	on	on	off	off	⋯	off	off	off	off	on
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
$\sum_{j=1}^{n}(V_{1,j}+V_{2,j}+V_{3,j})$	off	on	on	on	on	off	off	on	on	on	off	off	⋯	off	off	off	off	on
$V_{1,1}+\sum_{j=1}^{n}(V_{1,j}+V_{2,j}+V_{3,j})$	on	off	on	on	on	off	off	on	on	on	off	off	⋯	off	off	off	off	on

Table III. Proposed Algorithms and Their Related Parameters

Proposed algorithm	Magnitude of dc voltage sources	N_{level}	$V_{o,max}$	V_{block}
First proposed algorithm (P_1)	$V_{1,j}=V_{2,j}=V_{3,j}=V_{dc}$ for $j=1,2,\cdots,n$	$6n+3$	$(3n+1)V_{dc}$	$(21n+6)V_{dc}$
Second proposed algorithm (P_2)	$V_{1,1}=V_{2,1}=V_{3,1}=V_{dc}$, $V_{1,j}=V_{2,j}=V_{3,j}=2V_{dc}$ for $j=2,3,\cdots,n$	$12n-3$	$6n-2$	$(40n-13)V_{dc}$
Third proposed algorithm (P_3)	$V_{1,1}=V_{2,1}=V_{3,1}=V_{dc}$, $V_{1,j}=\frac{1}{3}V_{2,j}=V_{3,j}=3^{j-2}V_{dc}$ for $j=2,3,\cdots,n$	$5(3^{n-1})+4$	$\left[\frac{5(3^{n-1})+3}{2}\right]V_{dc}$	$[82(3^{n-1})-7]V_{dc}$
Fourth proposed algorithm (P_4)	$V_{1,j}=0.5V_{2,j}=V_{3,j}=2^{j-1}V_{dc}$ for $j=1,2,\cdots,n$	$2^{n+3}-5$	$(2^{n+2}-3)V_{dc}$	$[7(2^{n+2})-22]V_{dc}$

where n is the number of series-connected basic units. As the unidirectional power switches are used in the proposed cascaded multilevel inverter, the number of power switches is equal to the numbers of IGBTs, power diodes, and driver circuits. The other main parameter in calculating the total cost of the inverter is the maximum amount of blocked voltage by the switches. If the values of the blocked voltage by the switches are reduced, the total cost of the inverter decreases [12]. In addition, this value has the most important effect in selecting the semiconductor devices because this value determines the voltage rating of the required power devices. Therefore, in order to calculate this index, it is necessary to consider the amount of the blocked voltage by each of the switches. According to Fig. 5(b), the values of the blocked voltage by switches are equal to

$$V_{S'1} = V_{S'2} = V_{1,1} \quad (4)$$

$$V_{S1,j} = V_{S3,j} = \frac{V_{1,j} + V_{2,j} + V_{3,j}}{2} \quad (5)$$

$$V_{S4,j} = V_{S2,j} = V_{2,j} \quad (6)$$

$$V_{S5,j} = V_{1,j} + V_{2,j} + V_{3,j} \quad (7)$$

$$V_{T1} = V_{T2} = V_{T3} = V_{T4} = V_{o,\max} \quad (8)$$

Where $V_{o,max}$ is the maximum amplitude of the producible output voltage.Therefore the maximum amount of the blocked voltage in the proposed inverter V_{block} is equal to

$$V_{\text{block}} = \sum_{j=1}^{n} V_{\text{block},j} + V'_{\text{block}} + V_{\text{block,H}}. \quad (9)$$

In (9), $V_{block,j}$, V'_{block}, and V_{block}, H indicate the blocked voltage by the jth basic unit, the additional dc voltage sources, and the used H-bridge, respectively.

In the developed inverter, the number and maximum amplitude of the generated output levels are based on the value of the used dc voltage sources. Therefore, four different algorithms are proposed to determine the magnitude of the dc voltage sources. These proposed algorithms and all their parameters are calculated and shown in Table III. According to the fact that th magnitudes of all proposed algorithms except the first algorithm are different, the proposed cascaded multilevel inverter based on these algorithms is considered an asymmetric cascaded multilevel inverter. In addition, based on

the equations of the maximum output voltage levels and its maximum amplitude, it is clear that these values in the asymmetric cascaded multilevel inverter are more than those in the symmetric cascaded multi level inverters with the same number of used dc voltage sources and power switches.

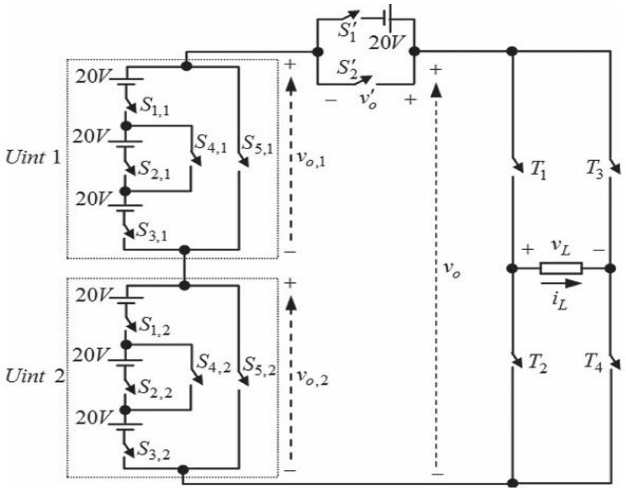

Fig7. Cascaded 15-level inverter based on the proposed basic unit.

In order to clarify the correct performance of the developed proposed inverter in generating the desired output voltage levels, the experimental results have been used. The number of required power electronic devices in the proposed inverter is completely based on the selected algorithm to determine the magnitude of the dc voltage sources. In this section, the investigations are done on a cascaded multilevel inverter that is shown in Fig. 3.4 This inverter consists of two proposed basic units and one additional series-connected dc voltage source that lead to the use of 7 dc voltage sources and 12 unidirectional power switches. The first proposed algorithm is considered to determine the magnitude of the dc voltage sources with Vdc =20 V. According to (5), this inverter is able to generate 15 levels (seven positive levels, seven negative levels, and one zero level) with the maximum amplitude of 140 V at the output. It is important to note that the used IGBTs on the prototype are BUP306D (with an internal anti parallel diode). The 89C52 microcontroller by ATMEL Company has been used to generate all switching patterns. In all processes of the experimental performance, the load is assumed as a resistive–inductive (R−L) load, with R=70 Ω, and L=55 mH. It is important to point out that the used control method in this inverter is the fundamental control method. The main reason to select this control method is its low switching frequency compared with other control methods that leads to reduction in switching losses.

IV. INDUCTION MOTOR

Induction Motor (1M) An induction motor is an example of asynchronous AC machine, which consists of a stator and a rotor. This motor is widely used because of its strong features and reasonable cost. A sinusoidal voltage is applied to the stator, in the induction motor, which results in an induced electromagnetic field. A current in the rotor is induced due to this field, which creates another field that tries to align with the stator field, causing the rotor to spin. A slip is created between these fields, when a load is applied to the motor. Compared to the synchronous speed, the rotor speed decreases, at higher slip values. The frequency of the stator voltage controls the synchronous speed [12]. The frequency of the voltage is applied to the stator through power electronic devices, which allows the control of the speed of the motor. The research is using techniques, which implement a constant voltage to frequency ratio. Finally, the torque begins to fall when the motor reaches the synchronous speed. Thus, induction motor synchronous speed is defined by following equation,

$$Ns = 120f/p \quad (10)$$

Where f is the frequency of AC supply, n, is the speed of rotor; p is the number of poles per phase of the motor. By varying the frequency of control circuit through AC supply, the rotor speed will change.

V.SIMULATION RESULTS

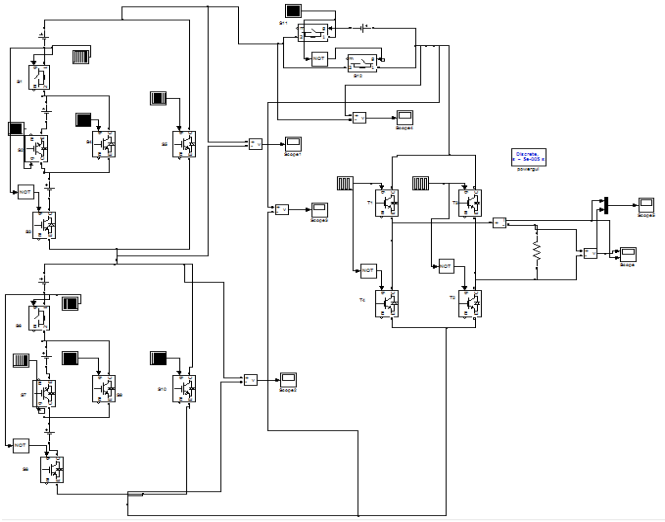

Fig.8.Simulink circuit for proposed 15 level inverter.

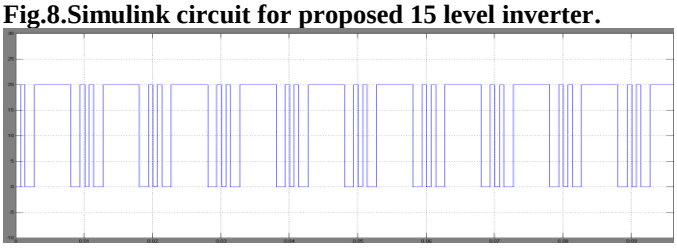

Fig.9.Simulation result for Vo.

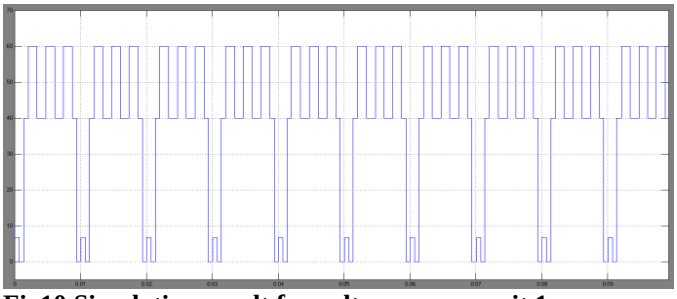

Fig10.Simulation result for voltage across unit 1.

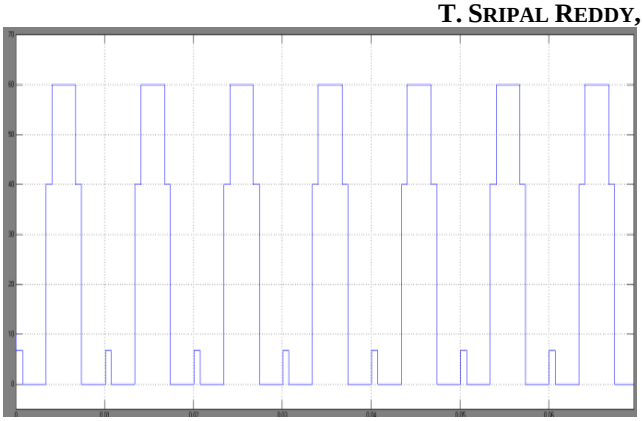

Fig.11.Simulation result for voltage across unit 2.

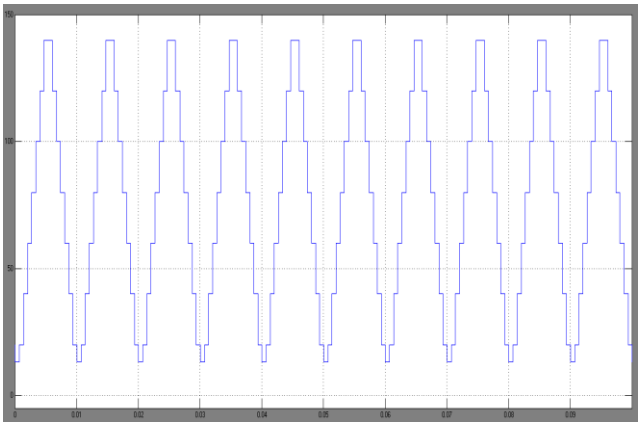

Fig.12.Simulation result for voltage across cascaded units.

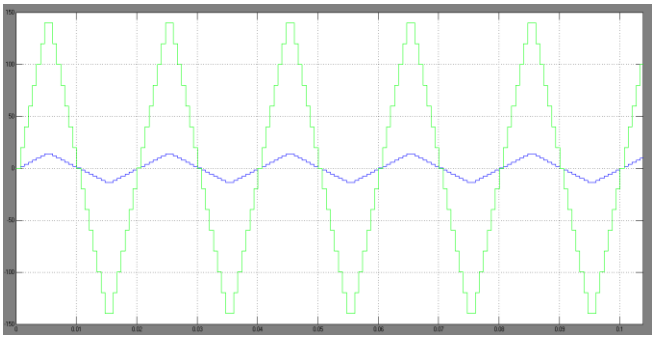

Fig.13.Simulation result for 15-level load voltage and load current.

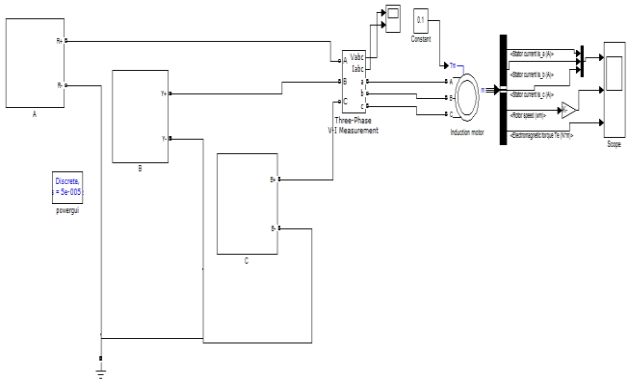

Fig.14.Simulink circuit for three phase 15 level inverter with induction motor drive.

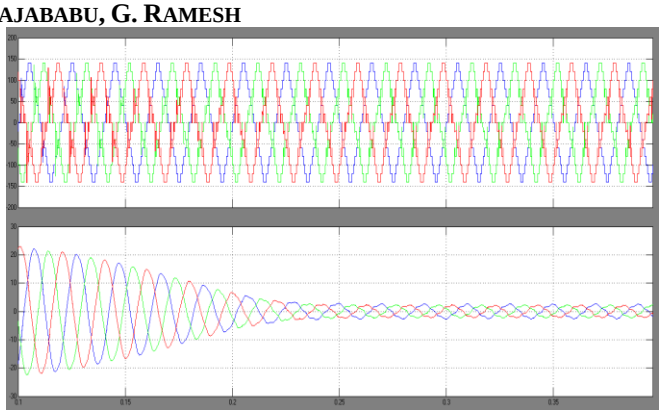

Fig.15.Simulation result for three phase voltage and current.

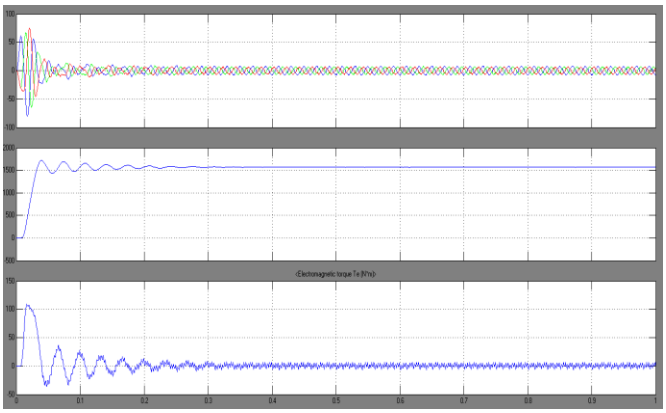

Fig.16.Simulation result for stator current, Speed and electromagnetic torque of induction motor.

VI. CONCLUSION

The simulation of 15-level multilevel inverter is successfully done with reduced number of switches. In this paper, a new basic unit for a cascaded multilevel inverter is proposed. By the series connection of several basic units, a cascaded multilevel inverter that only generates positive levels at the output is proposed. Therefore, an H-bridge is added to the proposed inverter to generate all voltage levels. This inverter is called the developed cascaded multilevel inverter. The several comparisons are done between the developed proposed single-phase cascaded inverter and its proposed algorithms with cascaded multilevel inverters that have been proposed in literature. Therefore, the developed proposed inverter has better performance and needs minimum number of power electronic devices that lead to reduction in the installation space and total cost of the inverter. Finally, the accuracy performance of the developed proposed single phase cascaded multilevel inverter in generating all voltage levels is verified by using the simulation results on a 15-level inverter. This inverter was developed to three phase system and performance of three phase induction motor has been checked successfully.

VII. REFERENCES

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