A Novel Low Cost Ultra-Thin chip Fabrication Technology

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Abstract: This paper proposes a new thin-chip fabrication technology, involving the preprocess module Chip film and the post process module Pick, Crack, and Place, presents a unique alternative to the established post process wafer thinning techniques for fabricating ultrathin silicon chips. In particular, the wafer preprocesses Chip film allows for low-cost fabrication of ultrathin chips with very accurate thickness control. The post process Pick, Crack, and Place is compatible with the conventional pick and place tools and provides mechanical support for the ultrathin chips at all stages of the chip fabrication and assembly process. System-in-foil and 3-D ICs based on the chip-to-wafer concept appear to be very favorable applications for this new technology.

Keywords: Image Silicon Wafer, Chip Fabrication, Ultra-Thin Chips, Low Cost.

I. INTRODUCTION

Silicon wafers [4] have been the building blocks of the electronic industry for more than 40 years. The silicon wafer [4] provides mechanical stiffness required for reliability in wafer processing and automated wafer handling. On the other hand, there are good reasons to look for possibilities to separate the thin electronic layer of a wafer from its bulk part. Recently there is an enormous growth in the diameter of wafer size. The primary reason for this increase was the need to ensure safe wafer manufacturing without breakage and to provide sufficient mechanical and thermal stability of the wafers in IC fabrication during processing steps of lithography and heat treatments. Beyond this, silicon wafers also must meet certain defect kinetic properties in device processing, which depend on the wafer thickness as well and are crucial for device yield and economic feasibility. Ultrathin [3], silicon chips will be an enabler for numerous emerging applications of silicon technology. Ultra-thin chip technology [6] and applications are to emerge as a new paradigm of silicon technology. Extremely thin and thus flexible silicon chips are expected to greatly enhance the emerging thin-film and organic semiconductor technologies by combining the well-known high performance of silicon chip technology with the large area and system-in-foil (SiF) applications.

Finally, there are likely numerous new applications in Microsystems that will emerge with the availability of ultra-thin chips. However, ultra-thin chip technology features not only a new paradigm due to the thus emerging applications, but also because the fabrication of thin silicon chips will require certain adjustments and innovations in silicon process technology and circuit integration: Ultra-thin silicon chips need to have very high edge and surface qualities, in order to retain the excellent inherent mechanical properties of silicon. The effect of stressors in increasing carrier mobility in the channel region of CMOS [1] transistors will likely be different for extremely thin compared to thick silicon substrates. Also, ultra-thin chips will have physical properties that are different from those found on thick bulk substrates. Transistors on thin chips under variable bending stress will suffer from the piezo resistive effect shifting their operating point, which is thus an additional aspect to be considered in circuit design. Finally, for economic reasons, the techniques used to fabricate an ultra-thin chip will have to be optimized in terms of minimizing the density of defects to a tolerable level. The enormous potential of integrated circuits(IC) [2] was recognized early by Intel co founder Gordon Moore in his visionary. It recognized that permanent cost reduction and steady development of wafer technology together play the key role.

The validity of Moore’s law has resulted in chips with a complexity and performance that had previously been inconceivable and with prices similar to common consumer goods. Advanced microprocessors contain more than one billion transistors on a silicon chip with an area of about 1 cm2. For decades Moore’s law has been established as a realistic guideline for development in the semiconductor industry. It forms the basis for the widely accepted technology roadmap, the International Technology Roadmap for Semiconductors (ITRS) for the semiconductor community. The ITRS defines a set of technological requirements per device generation considered necessary to enable further miniaturization.

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Fig. 1. Consequences of Moore’s law: price decay and wafer diameter.

More predicted a progressive increase in integration density and simultaneous reduction of unit costs per circuit component. Moore’s statement – known as Moore’s law today – hypothesized that the density of components would be doubled every 2 years, a statement that has been valid for more than 40 years. The significant enlargement of wafer size by a factor of 35 from 2-in. to 300-mm diameter contributed an additional important element to enhancement of productivity in device fabrication and lower total costs (Fig.1). This paper proposes a fabrication technology of ultra-thin chips using silicon wafer. The rest of the paper is organized as follows: section II gives the details about the fabrication technology. It also gives the details about the Wafer Thinning Technologies for Different Thickness Ranges. Section IV gives the complete details about the proposed new chip fabrication technique. Results for this approach are shown in section V and finally the conclusions are provided in section VI.

II. BASICS ABOUT FABRICATION

The recently increasing drive toward smaller thickness is motivated by new applications of silicon chip technology, which rely on mechanical flexibility, assembly on non-flat surfaces and chip stacking. Such thin wafers (100–300 mm) are mechanically stiff but tend to fracture and thus have to be handled with great care. Below 100 mm they become even more fragile and in addition start to bend under their own weight. In the thickness range 50–100 mm, fracture of wafers can be initiated even by small deflections. Below 50 mm wafers and chips become flexible, i.e., they remain intact also with a considerable degree of deflection applied. At 10 mm and smaller thicknesses they could tolerate bending radii of the order of 1 mm and less, which is out of the range of practical application. Such ultra-thin chips are in principle unconditionally stable, flexible and reliable. Conventional wafer grinding and chip dicing, however, introduces crystalline defects and micro cracks at a considerable level. Therefore, new techniques such as dicing-by-grinding are adopted to prevent edge chipping effects during chip dicing technology targeted at fabrication of ultra-thin [3] chips.

In general, different fabrication methods for thin wafers and chips (Fig. 2) offer prospects for the new applications of silicon technology, exploiting the unique features of ultra-thin chips under the economic constraints of the semiconductor industry.

Fig. 2. Illustrative comparison of generic subtractive technologies and one additive process

Wafer thickness of 150 mm is common and widespread and can be manufactured using standard grinding methods and equipment. Below 150 mm according wafer support is inevitable for a safe handling. Depending on wafer properties such as bow and warp, the structure and composition of active layers including topology and edge profile, wafers can be moved and processed on low cost grinding foils down to a thickness of 30 mm. However, the wafer does not only have to be stabilized for transport after thinning, but also during the complete wafer thinning process. The total process of wafer process is shown in figure 4.

Fig. 3 Flexible 50 mm wafer

Wafer thinning encompasses several steps: lamination of a grinding tape on the active side of the wafer (protection from process chemistry and mechanical carrier), multi grinding step (coarse and fine grinding), and stress relief (chemical-mechanical polishing or, alternatively, wet or dry etching), wafer mounting onto dicing foil and film frame carrier and grinding tape removal. The process sequence requires continuous handling of the thin wafer on a substrate. The thinning process module is fully integrated into a general purpose wafer treatment flow that enables the
delivery of known good (tested) ultra-thin dies (Fig.4). The process flow concept tolerates variations like wafer test after wafer thinning, separation on specialized probing equipment as well as laser separation of wafers.

Fig.4 Thin wafer process from wafer test to wafer separation

III. DESIGN APPROACH

This section gives the newly proposed wafer processing technology. A primarily new thin-chip fabrication process technology that services an improver method to define the final chip thickness in contrast to wafer thinning is subtractive by environment. While wafer thinning is a post process, the new technology here consists of a preprocess module Chip film and a post process module Pick, Crack, and Place.

A. Preprocess

Those preprocessed Chip film wafers are introduced to CMOS [1] device integration like any conventional bulk substrate with the sole difference that a coarse alignment of the CMOS [1] features to the dedicated chip areas needs to be arranged. This can be achieved either by a global alignment in the lithographic stepper tool or by using a zero-level alignment mark on the Chip film wafers.

After the CMOS fabrication is completed trenches are etched at the periphery of the chip areas down into the buried cavities, while small anchors are left to the bulk substrate at selected places, such as the chip corners. The trench etching thus leads to a transition from strong connections between chip and bulk wafer along the entire perimeter to a weak attachment only at those anchor points. The anchors are designed to be sufficiently strong for keeping the chips reliably in place during wafer handling but weak enough to allow for breaking off the chips by reasonable mechanical force. Next, to prepare for the buried cavity formation, an anodic etching step is carried out to form dual-layer porous silicon, consisting of a 1.5-mm fine porous layer above a 0.3-mm coarse porous layer. Good control of the porosity and thickness of those layers is a prerequisite for a reliable formation of a continuous buried cavity within the chip area. If the porosity were too large the fine porous layer above could collapse during the sintering, or irreversible bonding to the substrate could take place, possibly preventing simulation of the thin chips or causing damage to the chips during Pick, Crack & Place.

B. Post process

After CMOS circuit integration has been finished the chips are still firmly attached to the substrate at the perimeter. In such a state they cannot be detached from the substrate without being mechanically destroyed. The lateral connection to the substrate must therefore be weakened. This is achieved by reactive ion etching (RIE) deep trenches at the chip edges with use of the ‘Bosch processes, described in. The trenches need to extend down to the buried cavities. Only at the corners, or any other selected small region at the perimeter, trench formation is avoided so that lateral anchors remain after trenching.

Fig 6. Picks Crack and Place

This number of anchors are using for conventional pick-and-place assembly equipment. Since, in addition, breakage of the anchors is involved; the process is called Pick, Crack and Place. The maximum force to be applied is proportional
to the chip area. Therefore, the number and the size of the anchors need to be adjusted to the size, shape and thickness of the chips. The anchor type and optimum design were explored through finite element (FEM) simulations. A maximum distance up to which the chips could move freely without breaking off the anchors was set as a constraint. Beyond that distance the anchors were expected to break reliably at a location restricted by design. In that way extension of secondary micro cracks into the chip area could be avoided the best-suited anchor design. This type of anchor emerges from a chip area with a rather steep angle, leading to the intended breaking points. Notably, the trench outside of the anchors does not extend over the full distance between chip and spacer region but is restricted to minimum size in order to ensure similar etch depths of trench and holes.

IV. RESULTS

This section gives the complete details about the operational description of proposed fabrication technology. The figure.7 shows the pictorial representation of the proposed approach. The step by step procedure illustrated in fig.8.

V. CONCLUSIONS

This paper proposed a new thin chip fabrication technology. It is completely illustrated in two steps, preprocess and post process respectively. The pre process implemented by chip film technology, post process is implemented by pick and place concept. The result shown in above section gives the pictorial representation of the proposed fabrication technology. This approach reduces the Interconnect wiring length, delay, cost of owner chip. It uses a mixed-signal (38000 digital and 2700 analog transistors) circuit was fabricated on both bulk wafers.

VI. REFERENCES


