AC–DC Converter for Semi-Bridgeless using Phase-Shifted Gating Technique

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Abstract: In this paper, a phase-shifted semi-bridgeless boost power-factor-corrected (PFC) converter is proposed to simplify the current-sensing technique for the semi-bridgeless PFC converter. The converter features high efficiency at light loads and low ac input lines, which is critical to minimize the charger size, charging time, and amount and cost of electricity drawn from the utility. The converter is applicable for automotive levels I and II but is ideally suited for level-I residential charging applications. A detailed converter description and steady-state operation analysis of this converter is presented. Experimental results of a prototype boost converter, converting the universal ac input voltage to 400 V dc at 3.4 kW, are given, and the results are compared with an interleaved boost converter to verify the proof of concept and the reported analytical work.

Keywords: AC–DC power converters, boost converter, bridgeless power factor correction (PFC), current sensing, plug-in hybrid electric vehicle (PHEV) charger

I. INTRODUCTION

PLUG-IN hybrid electric vehicle (PHEV) is a hybrid vehicle with a storage system that can be recharged by connecting a plug to an external electric power source. The charging ac outlet inevitably needs an onboard ac–dc charger with power factor correction (PFC) [1]. An onboard 3.3-kW charger could charge a depleted battery pack in PHEVs to 95% charge in about 4 h from a 240-V supply for a 10-kWh battery pack [2]. A variety of circuit topologies and control methods has been developed for PHEV battery chargers. The two-stage approach with cascaded PFC ac–dc and dc–dc converters is the common architecture of choice for PHEV battery chargers, where the power rating is relatively high, and lithium-ion batteries are used as the main energy storage system [3]. The single-stage approach is generally only suitable for lead-acid batteries due to a large low-frequency ripple in the output current. In the two-stage architecture, the PFC stage rectifies the input ac voltage and transfers it into a regulated intermediate dc-link bus. At the same time, PFC is achieved [4]. A boost-derived PFC topology operated in continuous conduction mode is used in this paper as the main candidate for the front-end ac–dc PFC converter for PHEV battery charging. The front-end candidate topologies in the boost-derived class include the following: the interleaved boost converter, the bridgeless boost converter, the dual-boost converter, the semi-bridgeless boost converter, and the proposed phase-shifted semi-bridgeless (PSSB) boost converter.

A. Interleaved PFC

The interleaved boost converter is shown in Fig. 1. This topology uses two boost converters in parallel operating 180° out of phase [5]–[7]. The input current is the sum of the two inductor currents. Because the inductor ripple currents are out of phase, they tend to cancel each other and reduce the input ripple current caused by the boost switching action. The interleaved boost converter has the advantage of parallel semiconductors. Furthermore, by switching 180° out of phase, it doubles the effective switching frequency and introduces a smaller input current ripple; thus, the input electromagnetic interference (EMI) filter can be smaller than a single PFC boost topology [8]–[10]. Finally, this converter features a reduced output capacitor high-frequency ripple. However, as with the
single PFC boost, the most significant drawback of this topology is the very high localized loss and the resultant heat management issue for the input diode bridge rectifiers.

**Fig.2 Bridgeless PFC boost topology.**

**Fig.3 Gating scheme for the bridgeless PFC boost topology illustrating the identical gating signals for both MOSFETs.**

**Fig.4 Dual-boost PFC topology.**

**B. Bridgeless PFC**

The bridgeless boost topology, as shown in Fig. 2, is the second topology considered for this application. The gates of the power train switches are tied together; thus, the gating signals are identical, as shown in Fig. 3. It avoids the need for the rectifier input bridge but maintains the classic boost topology [11]–[21]. It is an attractive solution for applications > 1 kW, where power density and efficiency are important. The bridgeless boost converter, which is also known as the dual-boost PFC converter, solves the problem of heat management in the input rectifier diode bridge, but it introduces increased EMI [22]–[24]. This is because the amplitude of the noise source applied to the stray capacitor from high-voltage dc bus and power ground is a lot higher in bridgeless PFC; as a result, the common-mode (CM) noise generated by bridgeless PFC is much higher than the conventional boost PFC topology [24]. Another disadvantage of this topology is the floating input line with respect to the PFC stage ground, which makes it impossible to sense the input voltage without a low-frequency transformer or an optical coupler.

**C. Dual-Boost PFC**

The dual-boost converter, as shown in Fig. 4, is an alternative adaptation of the bridgeless boost topology [25]. In this topology, the MOSFET gates are decoupled, enabling one of the switches to remain on and operate as a synchronous MOSFET for a half-line cycle. Fig. 5 shows the gating scheme for a dual-

**Fig.5 Gating scheme for the dual-boost PFC topology illustrating half-line cycle synchronous rectification.**

**Fig.6 Semi-bridgeless PFC boost topology.**

**D. Semi-Bridgeless PFC**

The semi-bridgeless configuration, as shown in Fig. 6, includes the conventional bridgeless topology with two additional slow diodes, namely, Da and Db that connect the input to the PFC ground. The slow diodes were added to address EMI-related issues [22], [23]. The current does not always return through these diodes; therefore, their...
associated conduction losses are low. This occurs since the inductors exhibit low impedance at the line frequency; thus, a large portion of the current flows through the MOSFET intrinsic body diodes. The semi-bridgeless configuration also resolves the floating input line problem with respect to the PFC stage ground. The topology change enables input voltage sensing using a string of simple voltage dividers.

E. Bridgeless-Derived Topology Current Sensing

Three unique current-sensing circuits (Methods 1–3) for the bridgeless PFC topology are shown in Fig.7 to sense the current in the MOSFET and diode paths separately, since the current path does not share the same ground during each half-line cycle [13], [26]. These methods are also applicable to the dual-boost and semi-bridgeless topologies discussed in Section I. Method 1 is the passive current-sensing method reported in [13], which requires three current-sensing transformers—one in series with each switch and a third in the positive dc rail to sense the combined current of the two diodes, and an additional signal transistor with its associated complex control circuitry.

As an alternative solution, Method 2 uses a simple, but expensive, Hall effect sensor to directly sense the input current. This solution is not desired for highly cost-sensitive applications, including PHEV chargers. Method 3 uses a differential-mode amplifier in series with the input. This method is relatively inexpensive. However, due to the high switching frequency and the high output voltage, a high CM voltage leads to problematic noise in the current signal. In addition, since the current-sensing voltage is low to minimize the power loss, the power factor can be degraded by the sensing noise. In the following section, a new PSSB boost PFC converter is proposed to simplify the current-sensing technique in the bridgeless ac–dc PFC converters while maintaining all the advantages of the existing solutions.

II. PROPOSED PHASE-SHIFTED SEMI-BRIDGELESS CONVERTER

The PSSB topology shown in Fig. 8 is proposed as a solution to simplify current sensing in bridgeless PFC boost applications using the current synthesizer sensing method [27]. The inductor current synthesizer technique is used to predict the boost inductor current by sensing the MOSFET current [28].

The proposed topology power train incorporates the decoupled MOSFET gates, similar to that of the dual boost, and uses two slow diodes (Da and Db), similar to that of the semi-bridgeless boost, to link the ground of the PFC to the input line. The gating signals for the MOSFETs are 180° out of phase, as shown in Fig. 9. The phase-shifted gating enables the usage of the advanced current synthesizing method, which cannot be used in either the bridgeless topology or the dual-boost topology because all controllers available for these topologies require full input current shape sensing. The proposed topology exploits the advantages of the bridge-less and semi-bridgeless boost PFC topologies. In particular, it features reduced EMI, high efficiency at light loads, and low lines, which is critical to minimize the charger size, cost, charging time, and amount and cost of electricity drawn from the utility. The proposed converter steady-state operation is given in the following section.
III. CONVERTER STEADY-STATE OPERATION

To analyze the circuit operation, the input line cycle is separated into positive and negative half-cycles, as explained in Section III-A and B. In addition, the detailed circuit operation depends on the duty cycle. Positive half-cycle operation is provided for $D > 0.5$ in Section III-C and $D < 0.5$ in Section III-D.

A. Positive Half-Cycle Operation

Referring to Fig. 8, during the positive half-cycle, when the ac input voltage is positive, Q1 turns on and current flows through L1 and Q1 and continues through Q2 and then L2, returning to the line while storing energy in L1 and L2. When Q1 turns off, the energy stored in L1 and L2 is released as current flows through D1, through the load, and returns through the body diode of Q2/partially through $D_b$ back to the input.

B. Negative Half-Cycle Operation

Referring to Fig. 8, during the negative half-cycle, when the ac input voltage is negative, Q2 turns on and current flows through L2 and Q2 and continues through Q1 and then L1, returning to the line while storing energy in L2 and L1. When Q2 turns off, the energy stored in L2 and L1 is released as current flows through D2, through the load, and returns split between the body diode of Q1 and $D_a$ back to the input.

C. Detailed Positive Half-Cycle Operation and Analysis for $D > 0.5$

The detailed operation of the proposed converter depends on the duty cycle. During any half-cycle, the converter duty cycle is either greater than 0.5 (when the input voltage is smaller than half of the output voltage) or smaller than 0.5 (when the input voltage is greater than half of the output voltage). The three unique operating interval circuits of the proposed converter are provided in Figs.10–12 for duty cycles larger than 0.5 during the positive half-cycle input. Waveforms of the proposed converter during positive half-cycle operation with $D > 0.5$ are shown in Fig. 13. To simplify the analysis, it is assumed that the current splits between the bridge diode, the body diode, and the MOSFET channel equally. The intervals of operation are explained here.

Interval 1 $[t_{0} - t_{1}]$: At $t_{0}$, Q1/ Q2 are on, as shown in Fig.10.During this interval, the current in series inductances L1 and L2 increases linearly and stores the energy in these inductors. The energy stored in $C_o$ provides energy to the load. The return current is split among $D_b$, $D_{q2}$, and Q2.

Interval 2 $[t_{1} - t_{2}]$: At $t_{1}$, Q1 is on, and Q2 is off, as shown in Fig. 11. During this interval, the current in series inductances L1 and L2 continues to increase linearly and store the energy in these inductors. The energy stored in...
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Fig.13 PSSB boost converter steady-state waveforms for D > 0.5.

Co provides the load energy. The return current is split only between Db and Dq2.

Interval 3 [t2–t3]: At t2, Q1/Q2 is on again, and interval 1 is repeated, as shown in Fig. 10. During this interval, the current in series inductances L1 and L2 increases linearly and stores the energy in these inductors. The return current is again split among Db, Dq2, and Q2.

Interval 4 [t3–t4]: At t3, Q1 is off, and Q2 is on, as shown in Fig. 12. During this interval, the energy stored in L1 and L2 is released to the output through L1, D1, partially Q2, Dq2, L2, and Db.

D. Detailed Positive Half-Cycle Operation and Analysis for D < 0.5

The three unique operating interval circuits of the proposed converter are given in Figs. 14–16 for duty cycles less than 0.5 during the positive half-cycle. The waveforms of the proposed converter during these conditions are shown in Fig. 17. The intervals of operation are explained here.

Interval 1 [t0–t1]: At t0, Q1/ Q2 are off, as shown in Fig. 14. During this interval, the energy stored in L1 and L2 is released to the output through L1, D1, partially Dq2, L2 and Db.

Interval 2 [t1–t2]: At t1, Q1 is on, and Q2 is off, as shown in Fig. 15. During this interval, the current in series inductances L1 and L2 increases linearly and stores the energy in these inductors. The energy stored in Co provides energy to the load. The return current is split only between Db and Dq2.

Interval 3 [t2–t3]: At t2, Q1/Q2 is off again, and interval 1 is repeated, as shown in Fig. 14. During this interval, the current in series inductances L1 and L2 decreases linearly, and the energy in these inductors are released. The energy stored in L1 and L2 is released to the output through L1, D1, partially Dq2, L2, and Db.

Interval 4 [t3–t4]: At t3, Q1 is off, and Q2 is on, as shown in Fig. 16. During this interval, the energy stored in L1 and L2 is released to the output through L1, D1, partially Q2, Dq2, L2, and Db.
The operation of the converter during the negative input voltage half-cycle is similar to the operation of the converter during the positive input voltage half-cycle. The estimated loss distribution of the semiconductors is provided in Fig. 18 at 70 kHz switching frequency, 240 V input, and 3300 W load for benchmark conventional boost and interleaved boost converters and the proposed PSSB boost converter.

IV. EXPERIMENTAL RESULTS

A prototype of the proposed PSSB boost PFC converter was built. In addition, prototypes of an interleaved boost converter and a semi-bridgeless boost converter were built to benchmark the proposed converter. The components used in experimental prototypes are provided in Table I.

<table>
<thead>
<tr>
<th>Devices</th>
<th>Designator</th>
<th>Part #</th>
</tr>
</thead>
<tbody>
<tr>
<td>Regular Diodes</td>
<td>Da,Db</td>
<td>25ETS088</td>
</tr>
<tr>
<td>Fast Diodes</td>
<td>D1,D2</td>
<td>1DB06S60C</td>
</tr>
<tr>
<td>MOSFETs</td>
<td>Q1,Q2</td>
<td>IPB60R099CP</td>
</tr>
</tbody>
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Fig. 17 PSSB boost converter steady-state waveforms for D < 0.5.

Fig. 18 Comparison of the estimated loss distribution in the semiconductors.

Fig. 19 (Top) Control board. (Bottom) Power board.

Fig. 20 Efficiency as a function of output power at Vin = 240 V, Vo = 400 V, and 70 kHz switching frequency.
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Fig. 19 shows the proposed phase-shifted bridgeless boost prototype. It consists of a control board and a power board attached to a heat sink with the PFC inductors. The experimental efficiency of the phase-shifted bridgeless boost converter, benchmark interleaved boost converter, and conventional bridgeless boost converter are provided in Fig. 20 for 240 V input and in Fig. 21 for 120 V input at 70 kHz switching frequency and 400 V output. The light-load efficiency of the proposed converter is significantly better than that of the benchmark interleaved boost PFC due to the absence of the input rectifier bridge. However, as the load increases, the efficiency drops due to additional heat dissipation in the intrinsic body diodes of the MOSFETs. A family of efficiency curves for the proposed converter versus output power at different line voltages is provided in Fig. 22. It is observed that a peak efficiency of 98.8% is achieved at 265 V input and 1000 W load. To verify the quality of the input current in the proposed converter, the measured input current total harmonic distortion (THD) is provided in Fig. 23. The mains current THD is less than 5% from half load to full load, and it is compliant with IEC 61000-3-2 (see Fig. 25).

Fig. 20

Fig. 21 Efficiency as a function of output power at Vin = 120 V, Vo = 400 V, and 70 kHz switching frequency.

Fig. 22 Efficiency as a function of output power at Vin = 120 and 240 V, Vo = 400 V, and 70 kHz switching frequency.

Fig. 23 PSSB measured THD as a function of output power at Vin = 120 and 240 V, Vo = 400 V, and 70 kHz switching frequency.

Fig. 24 PSSB measured power factor as a function of output power at Vin =120 and 240 V, Vo = 400 V, and 70 kHz switching frequency.
The PSSB measured power factor is provided in Fig. 24 over the entire load range for 120 and 240 V input. The power factor is greater than 0.99 from half load to full load. The PSSB harmonics are provided and compared with the EN 61000-3-2 class-D standard in Fig. 25. The proposed converter meets the class-D standard limits for all harmonics. Experimental waveforms from the proposed converter prototype are provided in Figs. 26–29. The input current, input voltage and output voltage are given in Fig. 26. As shown,

The input current is in phase with the input voltage and has a sinusoidal shape. Additionally, there is a low-frequency ripple on the output voltage, which is inversely proportional to the value of PFC bus output capacitors.

The inductor current, input current, and current sensed in the MOSFET through a current transformer are provided in Fig. 27. It is noted that during the positive half-cycle, the inductor current is the same as the input current. However, during the negative half-cycle, the input current is partially flowing through slow diodes Da and Db. The gating signals, sensed MOSFET current, and inductor current are provided for duty cycles less than 0.5 in Fig. 28 and greater than 0.5 in Fig. 29. These waveform shapes match the theoretical expected waveforms.

**CONCLUSION**

A high-performance PSSB ac–dc boost PFC converter topology has been proposed to simplify the current-sensing technique for the semi-bridgeless PFC converter. The converter features high efficiency at light-load and
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low-line conditions, which is critical to minimize the charger size, cost, charging time, and amount and cost of electricity drawn from the utility. The converter is ideally suited for automotive level-I residential charging applications in North America, where the typical supply is limited to 120 V and 1.44 kVA. An analysis and performance characteristics have presented. A prototype converter circuit was built to verify the proof of concept. Theoretical wave forms were presented and compared with the results taken from the prototype. Experimental results demonstrate that the mains input current THD is less than 5% from half load to full load, and the converter is compliant with the IEC 61000-3-2 class-D standard. The converter power factor was also provided at full load for 120 and 240 V input. The power factor is greater than 0.99 from 50% load to full load. The proposed converter achieves a peak efficiency of 98.8% at 265 V input and 1 kW output power.

REFERENCES


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